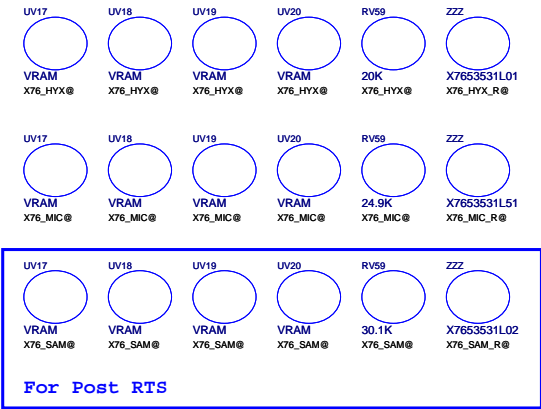


MODEL NAME : Marble Falls/ Discrete  
PROJECT CODE : ZAL50, ZAL60  
PCB NO : LA-B072P



# Dell / Compal Confidential

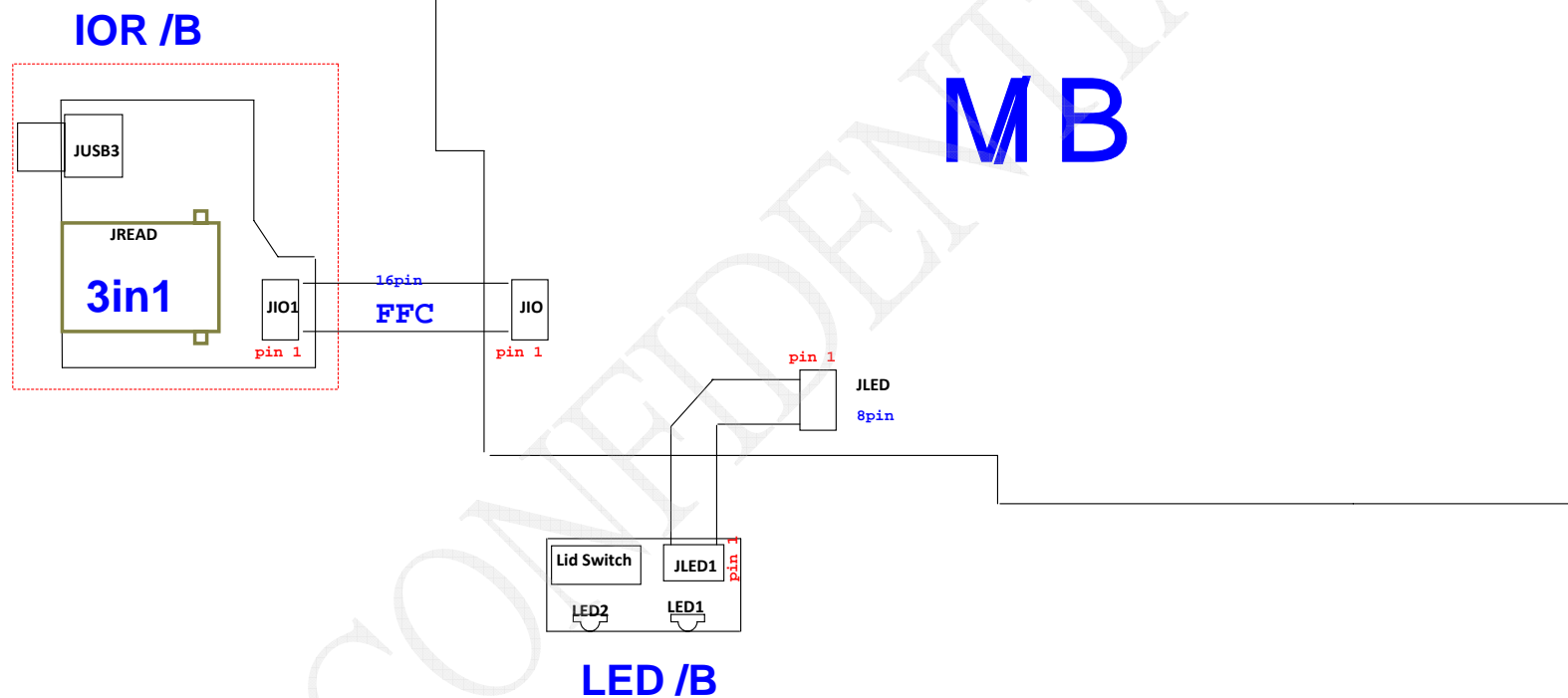
## Schematic Document

Intel Broadwell ULT  
Marble Falls 14"/15" Value  
DIS

2013-10-03 Rev: 0.1

|   |  |                    |                 |                              |                     |
|---|--|--------------------|-----------------|------------------------------|---------------------|
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|   |  |                    |                 | 4019RU                       | A                   |
|   |  |                    |                 | Date: Monday, April 07, 2014 | Sheet 1 of 54       |





|   |            |                    |            |                          |                        |
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|   |            |                    |            | Date:                    | Monday, April 07, 2014 |
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|   |            |                    |            | Rev                      | A                      |

## Board ID Table

### Phase ID

| RE79 | CE54  | REV |
|------|-------|-----|
| 240K | 4700p | X00 |
| 130K | 4700p | X01 |
| 62K  | 4700p | X02 |
| 33K  | 4700p | X03 |
| 8.2K | 4700p | A00 |
| 4.3K | 4700p |     |
| 2K   | 4700p |     |
| 1K   | 4700p |     |

BOARD ID rise time is measured from 5%~68%.

### Config ID

| RE89   | RE90   | Config   |
|--------|--------|----------|
| De-Pop | Pop    | Discrete |
| Pop    | De-Pop | UMA      |

### SMBUS Control Table

|                                  | SOURCE  | BATT | Charger | DDR3L | XDP | WLAN<br>NGFF | Touch<br>pad | VGA |
|----------------------------------|---------|------|---------|-------|-----|--------------|--------------|-----|
| CHARGER_SMBCLK<br>CHARGER_SMBDAT | MEC5085 |      | V       |       |     |              |              |     |
| PBAT_SMBCLK<br>PBAT_SMBDAT       | MEC5085 | V    |         |       |     |              |              |     |
| GPU_SMBCLK<br>GPU_SMBDAT         | MEC5085 |      |         |       |     |              |              | V   |
| SML1_SMBCLK<br>SML1_SMBDATA      | MEC5085 |      |         |       |     |              |              |     |
| SMBCLK<br>SMBDATA                | ULT     |      |         | V     | V   | V            | V            |     |
| SML0CLK<br>SML0DATA              | ULT     |      |         |       |     |              |              |     |
| SML1CLK<br>SML1DATA              | ULT     |      |         |       |     |              |              |     |

Link

### CLOCK SIGNAL

|              |                  |
|--------------|------------------|
| CLKOUT_PCIE0 |                  |
| CLKOUT_PCIE1 |                  |
| CLKOUT_PCIE2 | 10/100/1000 LAN  |
| CLKOUT_PCIE3 | NGFF (BT + WLAN) |
| CLKOUT_PCIE4 |                  |
| CLKOUT_PCIE5 |                  |

Symbol Note :



: means Digital Ground



: means Analog Ground

ULT

### USB3.0

|       |                 |
|-------|-----------------|
| Port1 | USB connector 1 |
| Port2 | USB connector 2 |
| Port3 |                 |
| Port4 |                 |

### USB2.0

|       |                        |
|-------|------------------------|
| Port0 | USB connector 1        |
| Port1 | USB connector 2        |
| Port2 | USB connector 3 (IO/B) |
| Port3 | Finger print           |
| Port4 | NGFF (BT + WLAN)       |
| Port5 | Touch Screen Panel     |
| Port6 | Card Reader            |
| Port7 | Camera                 |

### PCI EXPRESS

|        |                  |
|--------|------------------|
| Lane 1 |                  |
| Lane 2 |                  |
| Lane 3 | 10/100/1000 LAN  |
| Lane 4 | NGFF (BT + WLAN) |
| Lane 5 | PEG (N15S)       |
| Lane 6 |                  |

### SATA

|       |     |
|-------|-----|
| SATA0 | HDD |
| SATA1 |     |
| SATA2 |     |
| SATA3 |     |

### DDI

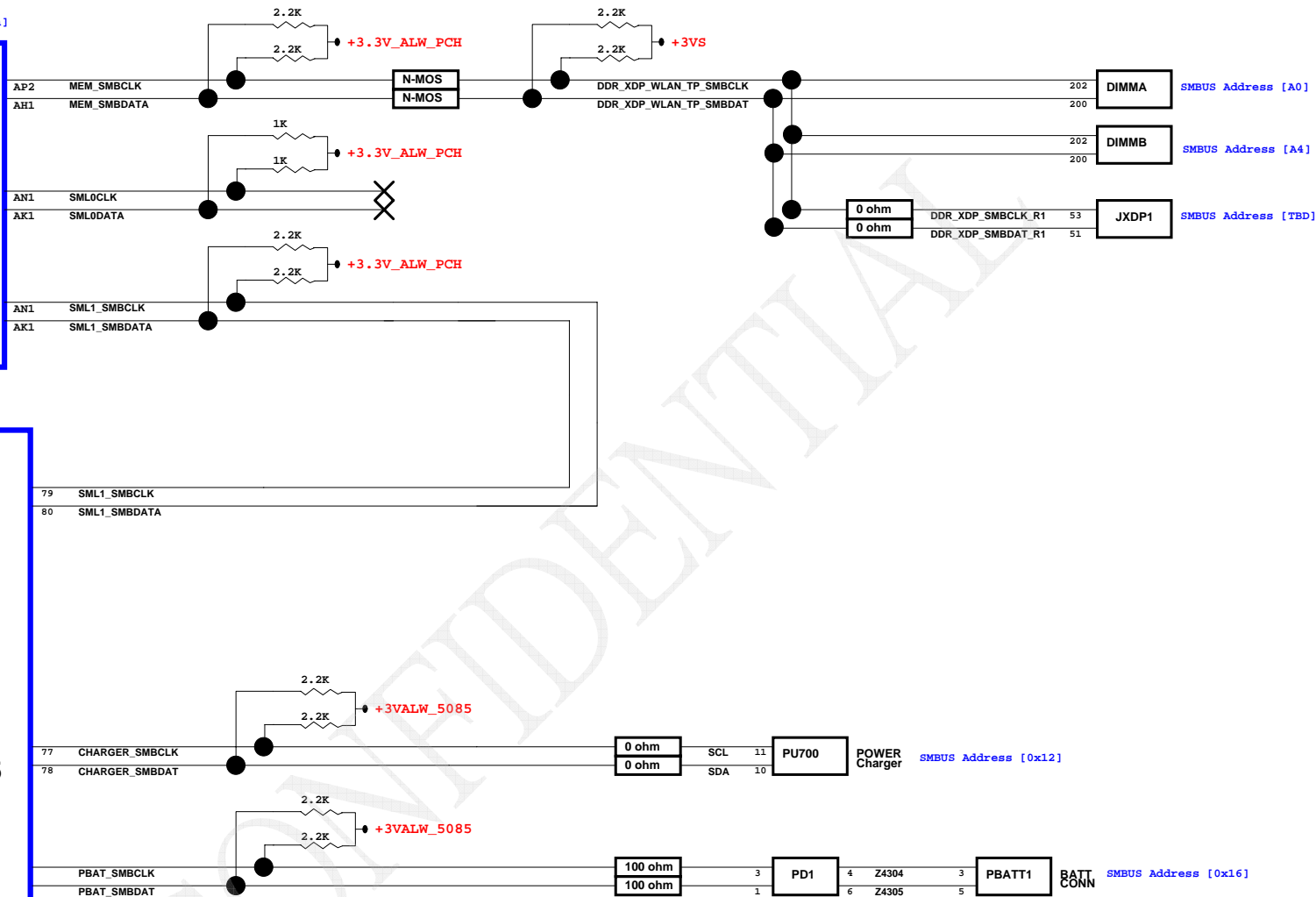
|      |           |
|------|-----------|
| DDI1 | HDMI      |
| DDI2 | DP to CRT |

|   |                    |                 |            |                          |                        |
|---|--------------------|-----------------|------------|--------------------------|------------------------|
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|   |                    |                 |            | Date                     | Monday, April 07, 2014 |
|   |                    |                 |            | Sheet                    | 4 of 54                |

SMBUS Address [0x9a]

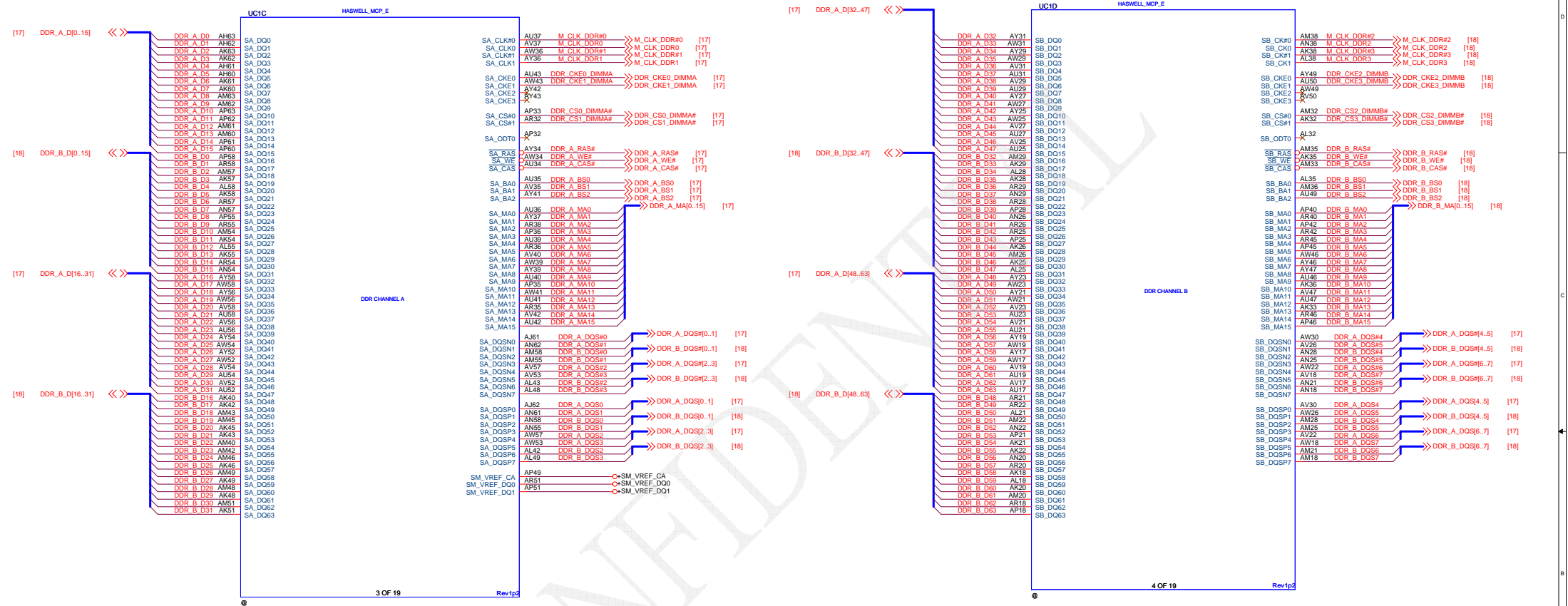
MCP

MEC 5085



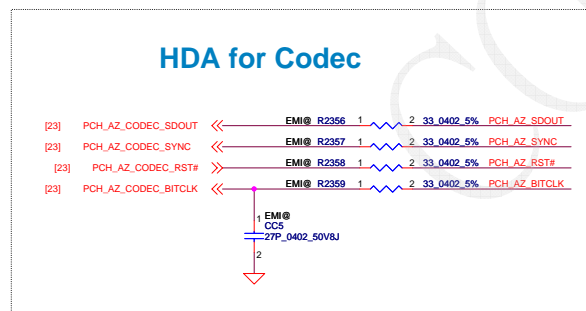
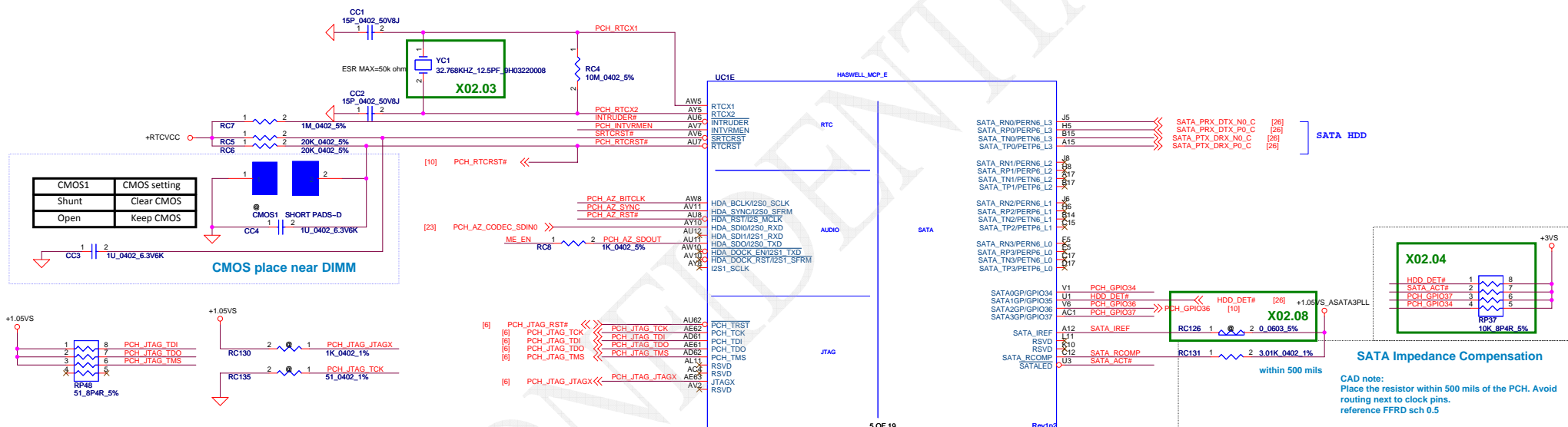
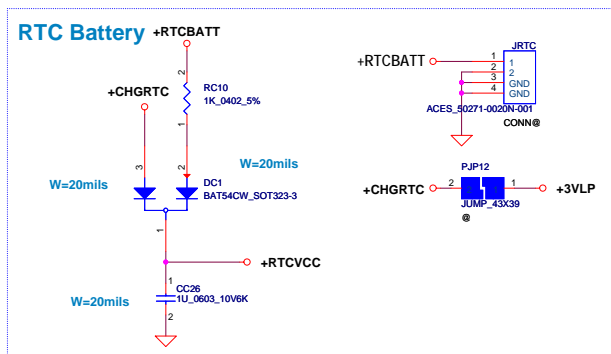


# Interleaved Memory



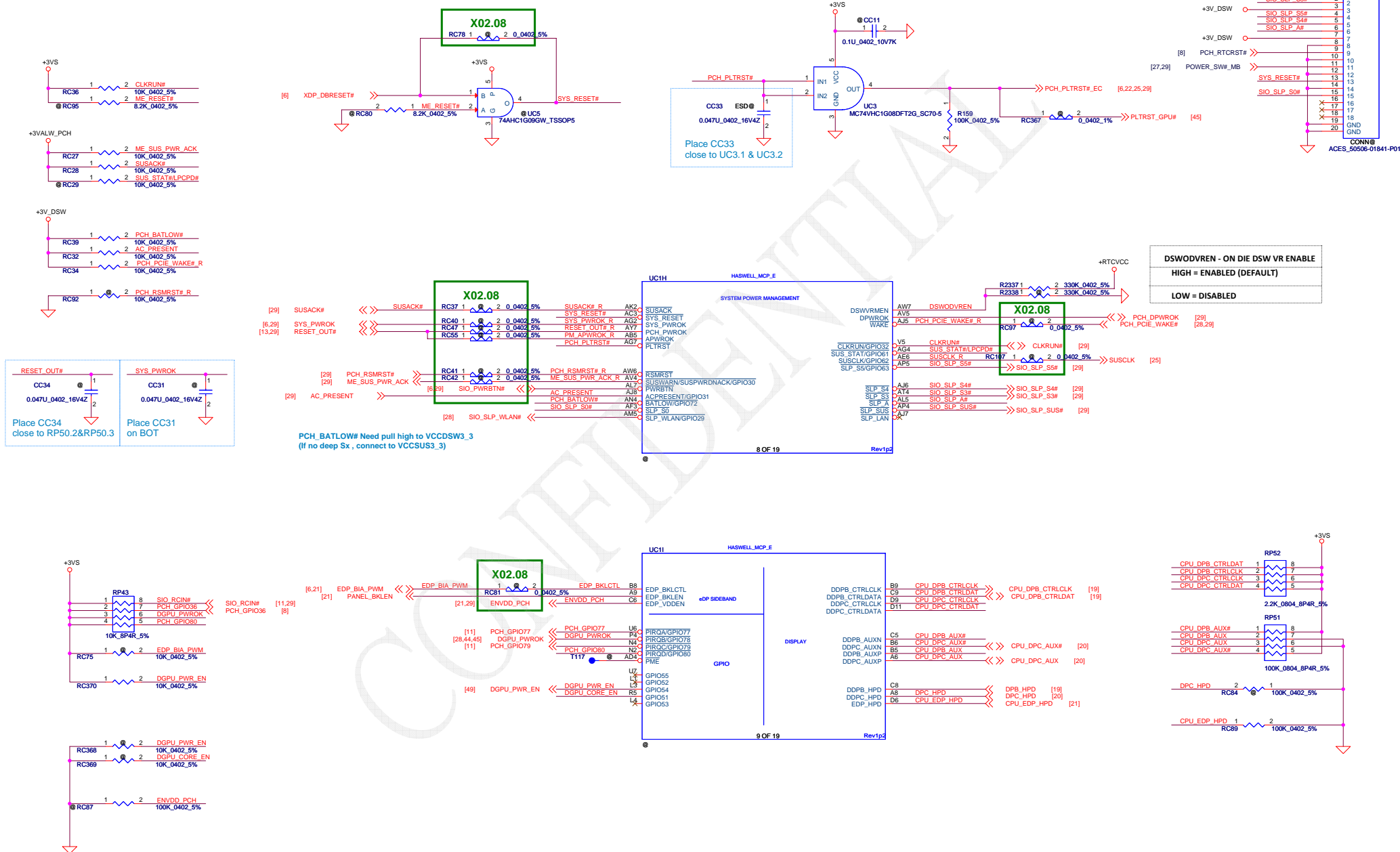
confirm by intel request PDG P141

|   |            |                    |            |                          |                        |
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|   |            |                    |            | Sheet                    | 7 of 54                |

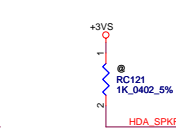
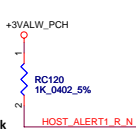
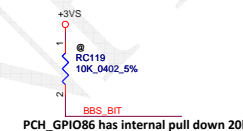
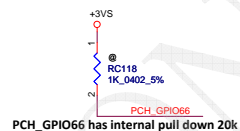
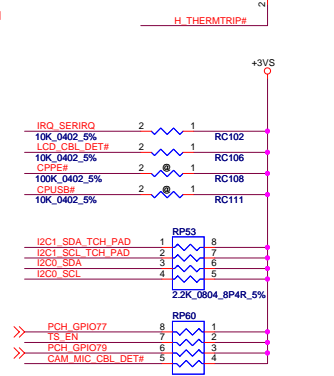
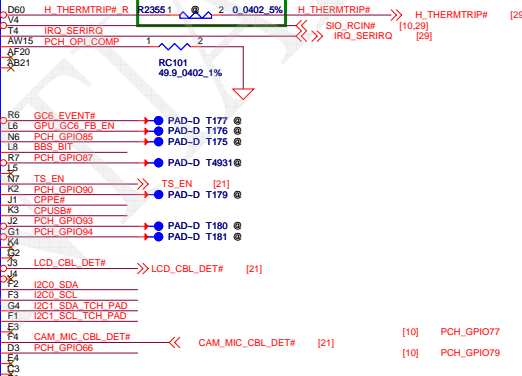
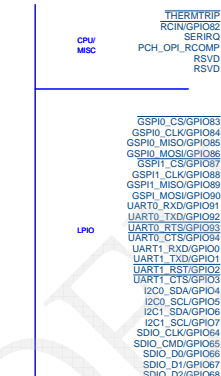
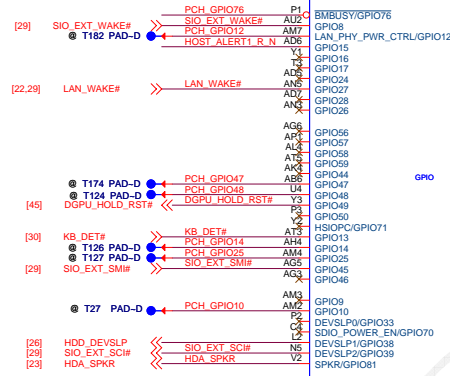
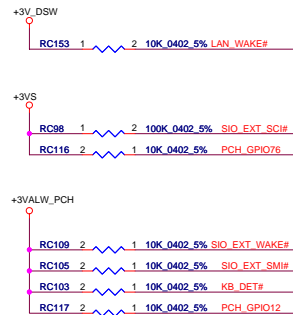








|   |            |                    |            |                 |                     |
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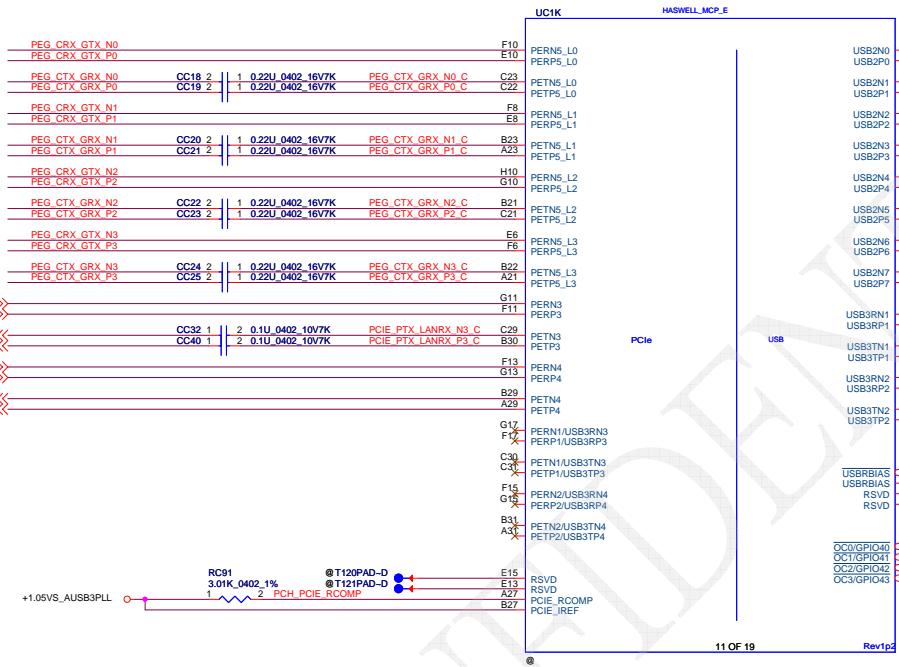
| GPIO66                     | GPIO86                  | GPIO15              | GPIO81          |
|----------------------------|-------------------------|---------------------|-----------------|
| TOP-BLOCK SWAP OVERRIDE    | BOOT BIOS STRAP BIT BBS | TLS CONFIDENTIALITY | NO REBOOT STRAP |
| HIGH depop RC118 (DEFAULT) | HIGH LOW(DEFAULT) LPC   | HIGH LOW(DEFAULT)   | disable         |
| LOW pop RC122              | LOW(DEFAULT) SPI        | LOW(DEFAULT)        | enable          |

[45] PEG\_CTX\_GRX\_P0[0..3] >> PEG\_CTX\_GRX\_P0[0..3]  
 [45] PEG\_CTX\_GRX\_N0[0..3] >> PEG\_CTX\_GRX\_N0[0..3]  
 [45] PEG\_CRX\_GTX\_P0[0..3] << PEG\_CRX\_GTX\_P0[0..3]  
 [45] PEG\_CRX\_GTX\_N0[0..3] << PEG\_CRX\_GTX\_N0[0..3]

LAN

NGFF WLAN

[22] PCIE\_PRX\_LANTX\_N3  
 [22] PCIE\_PRX\_LANTX\_P3  
 [22] PCIE\_PTX\_LANRX\_N3  
 [22] PCIE\_PTX\_LANRX\_P3  
 [25] PCIE\_PRX\_WLANTX\_N4  
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 [25] PCIE\_PTX\_WLANRX\_P4



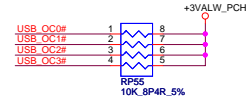
USB

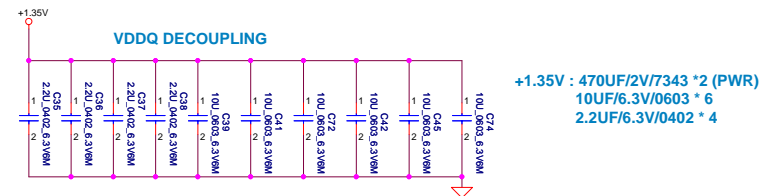
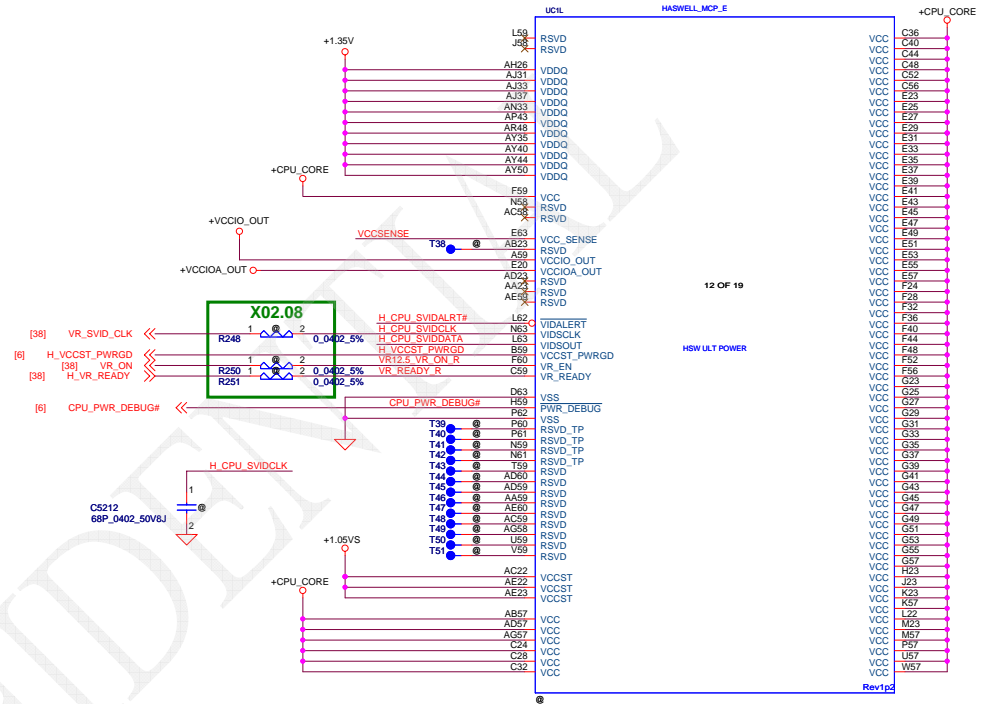
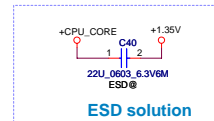
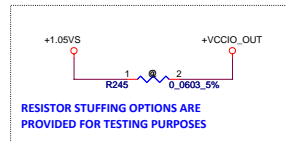
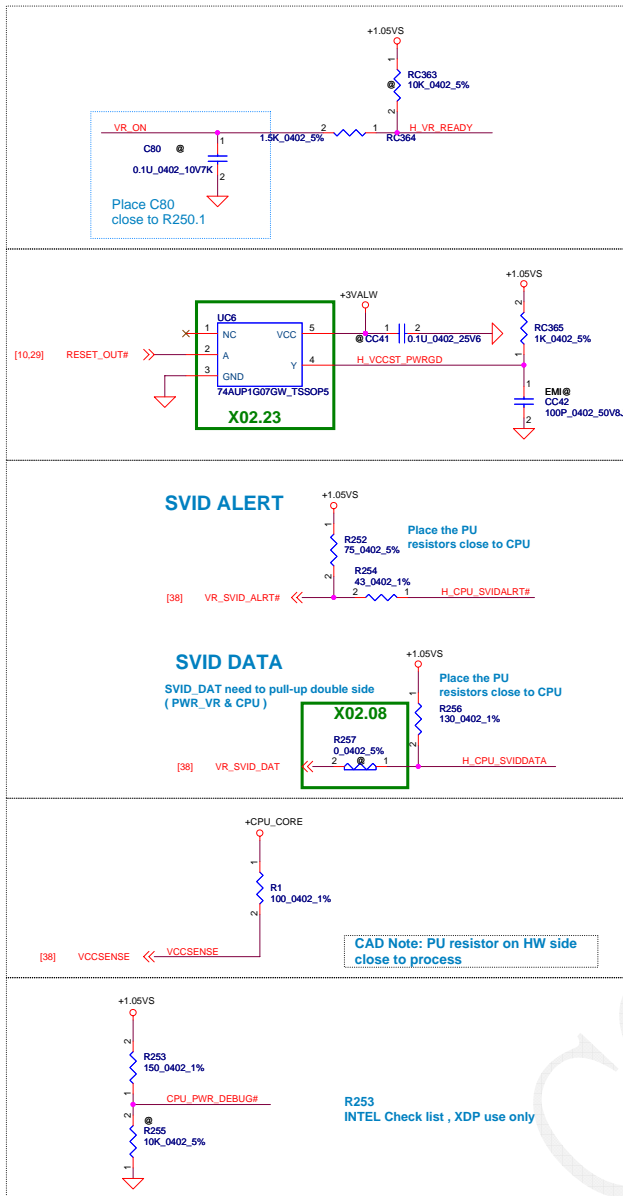
PCie

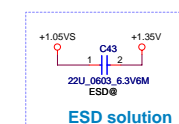
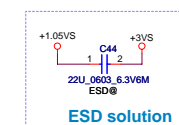
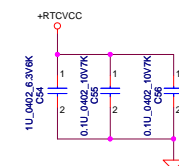
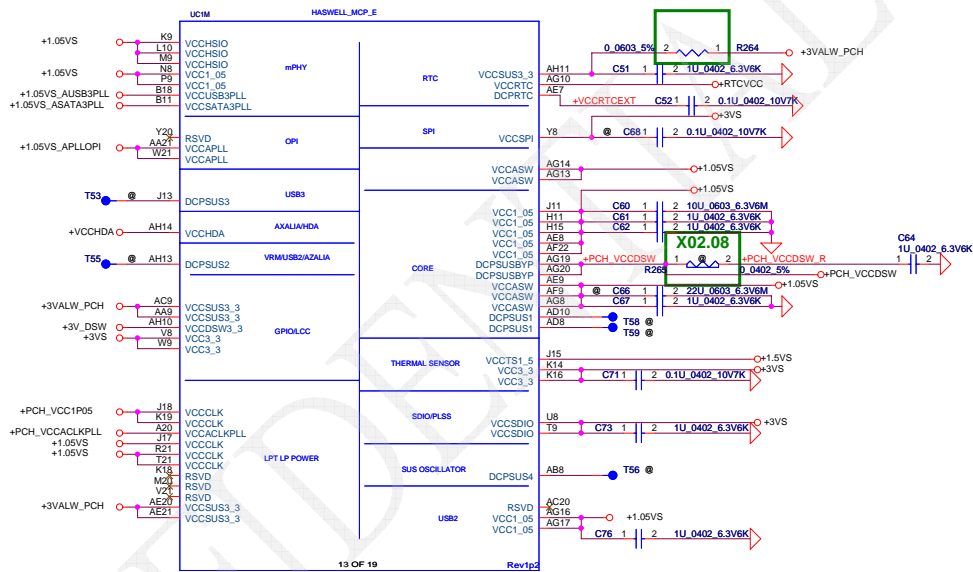
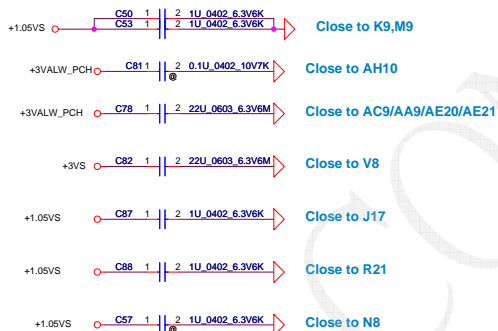
11 OF 19

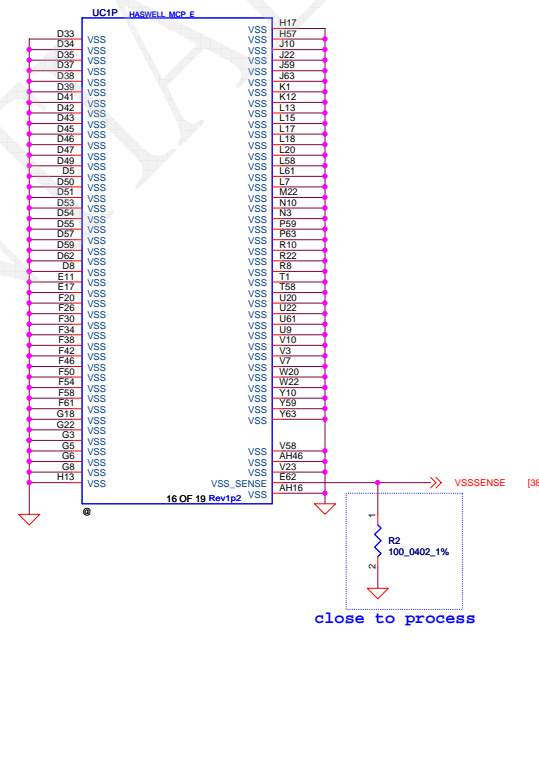
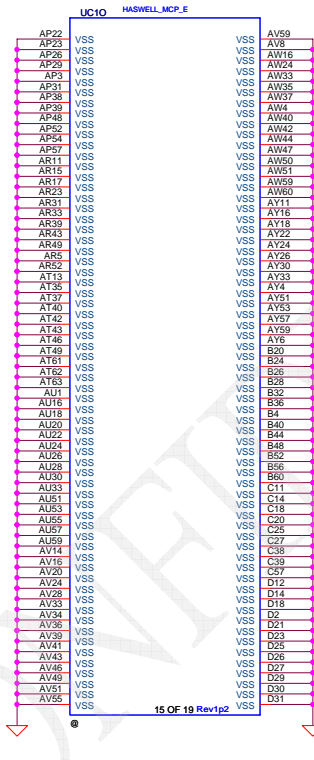
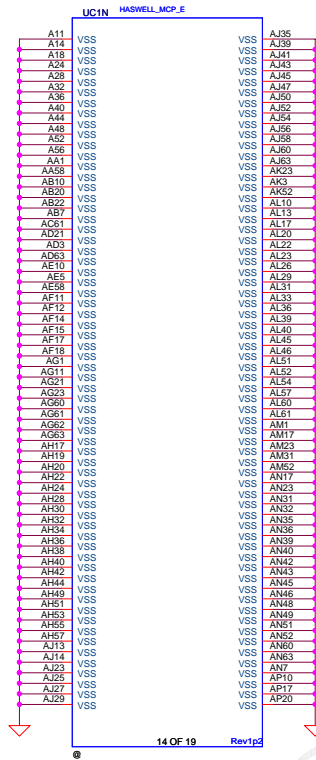
Rev1.0

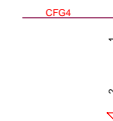
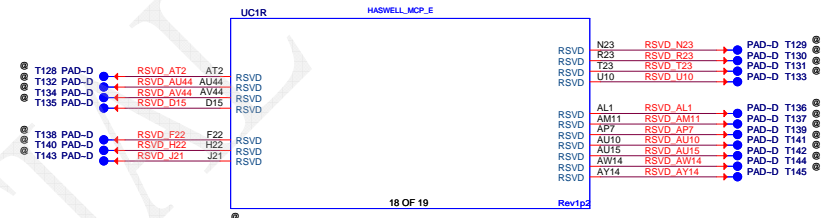
**CAD NOTE:**  
 Route single-end 50-ohms and max 500-mils length.  
 Avoid routing trace to clock pins or under stitching capacitors.  
 Recommended minimum spacing to other signal traces is 15 mils.











|      |  |
|------|--|
|      | Display Port Presence Strap  |
| CFG4 | 1 : Disabled; No Physical Display Port attached to Embedded Display Port               |
|      | 0 : Enabled; An external Display Port device is connected to the Embedded Display Port |

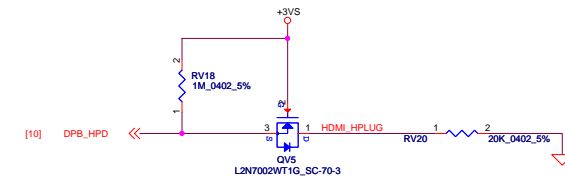
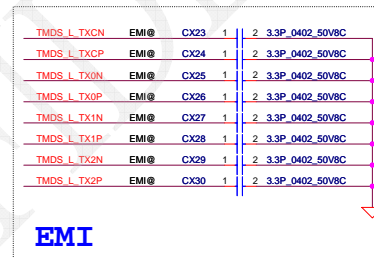
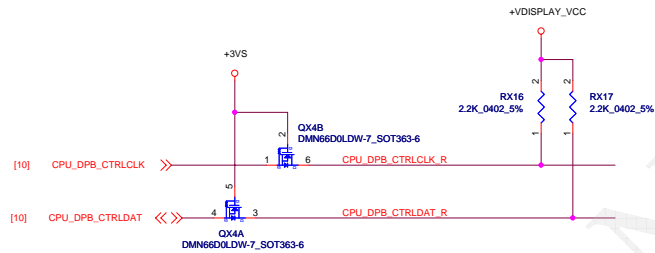
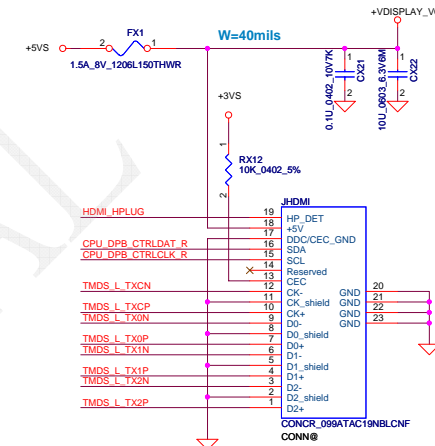
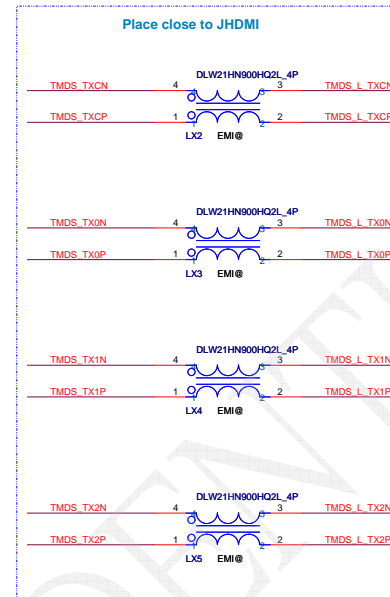
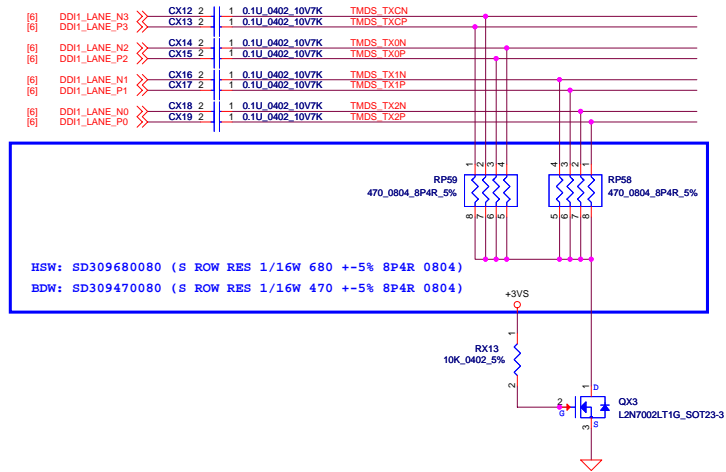


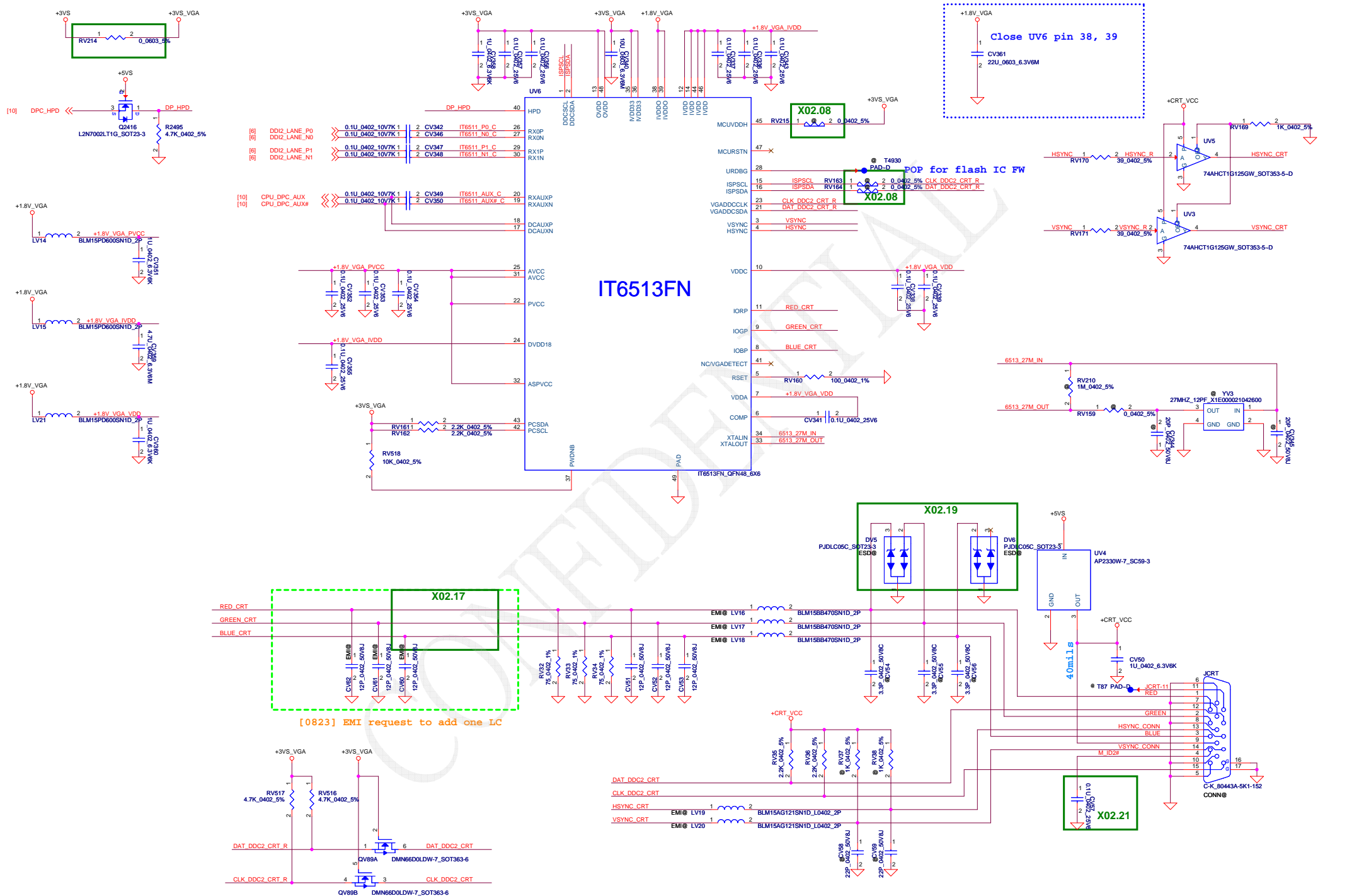
| EAR-STALL/NOT STALL RESET SEQUENCE AFTER PCU PLL IS LOCKED |   |
|--|---|
| CFG0   | 1:(Default) Normal Operation; No stall<br>0:Lane Reversed |



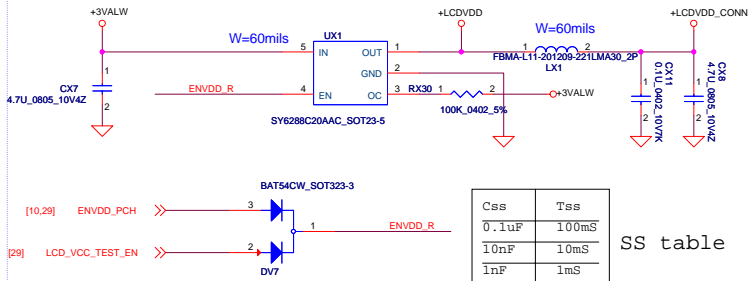






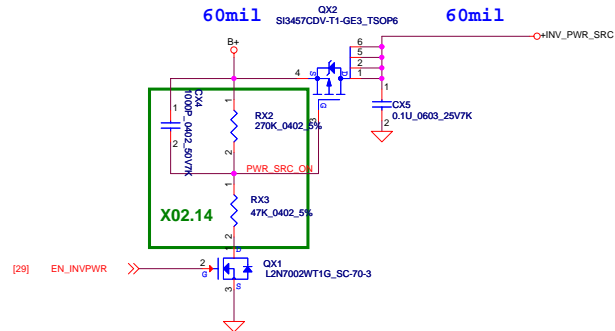


## LCD PWR CTRL



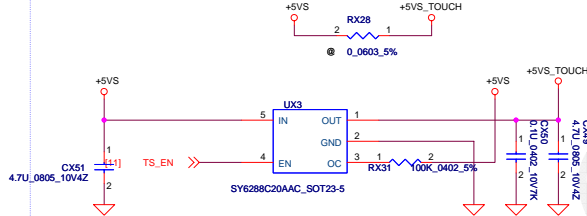
SS table

## LCD backlight PWR CTRL



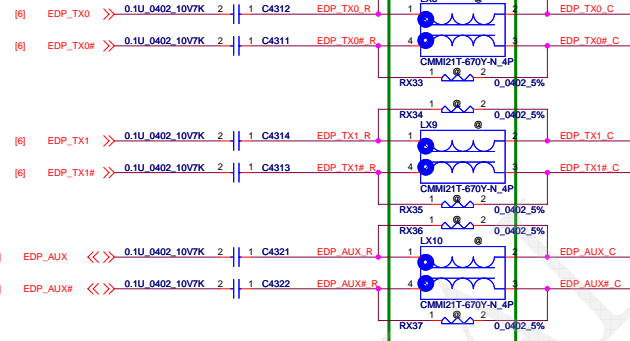
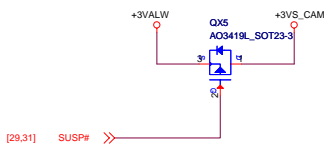
SS table

## \* Touch Screen Panel

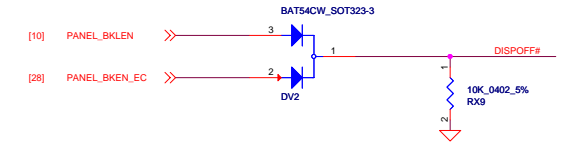
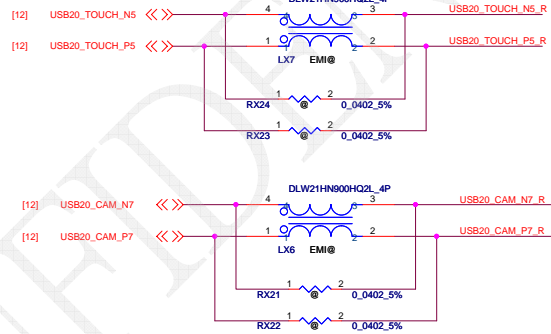
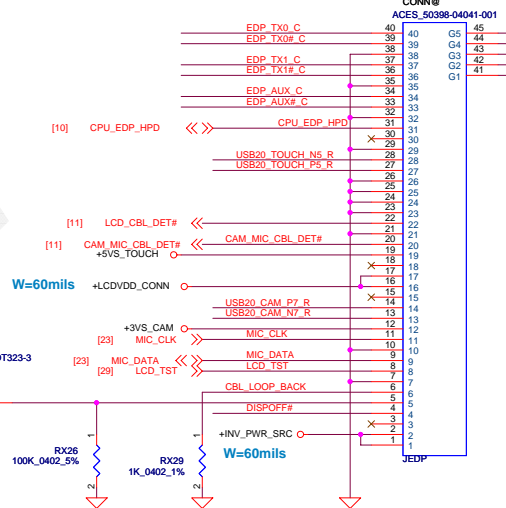


SS table

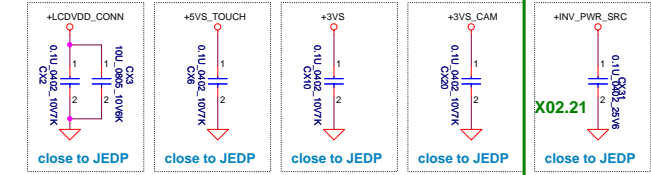
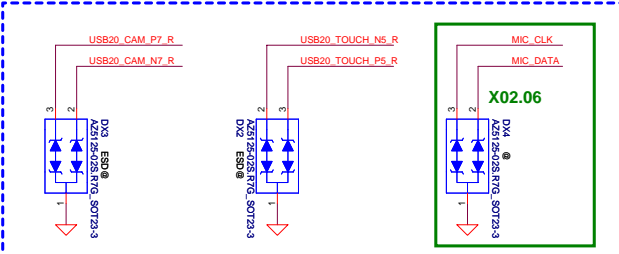
## Webcam PWR CTRL



## eDP Connector



## close to JEDP



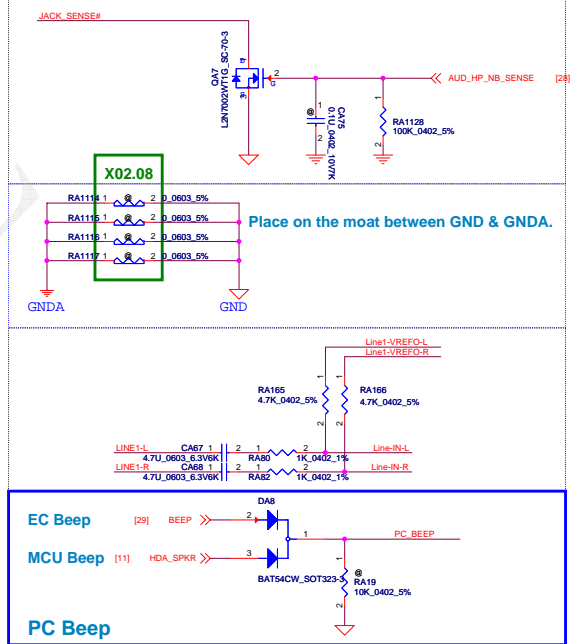
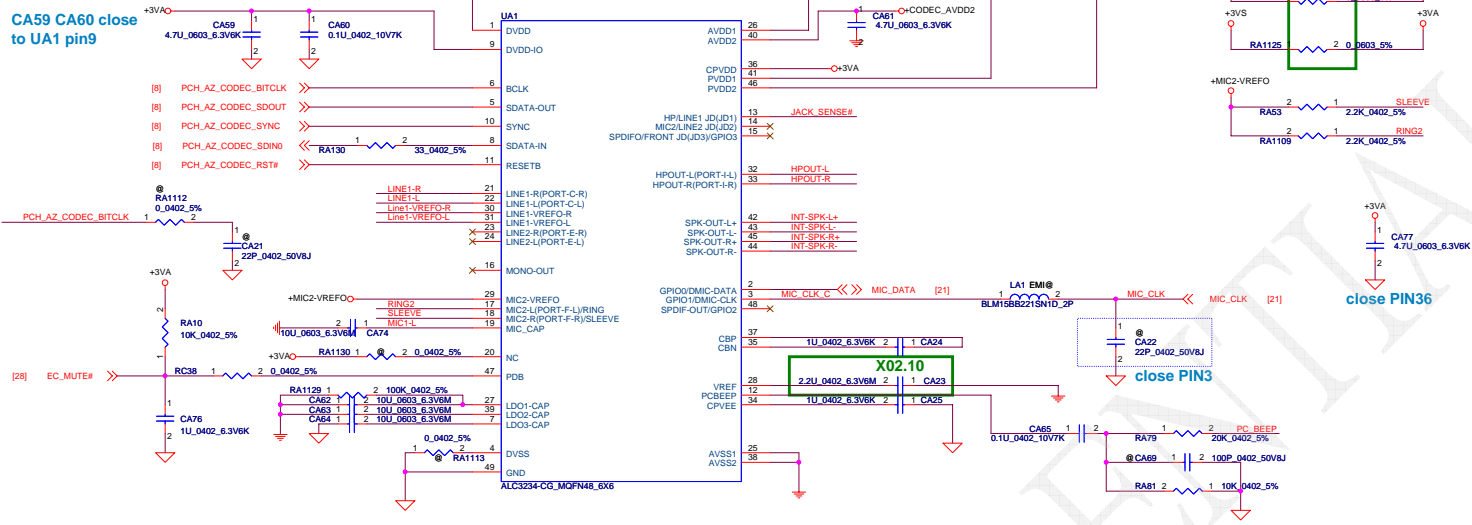


CA71, CA51 place close to Pin 26

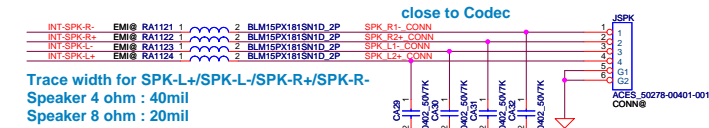
CA33, CA55 change Value  
from 10U\_0603\_6.3V6M to  
4.7U\_0603\_6.3V6K

CA57, CA58 close  
to UA1 pin1

CA59 CA60 close  
to UA1 pin9

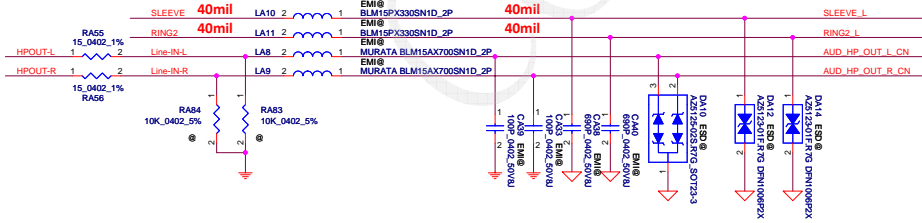


Close to UA1  
Pin11,13,14,16



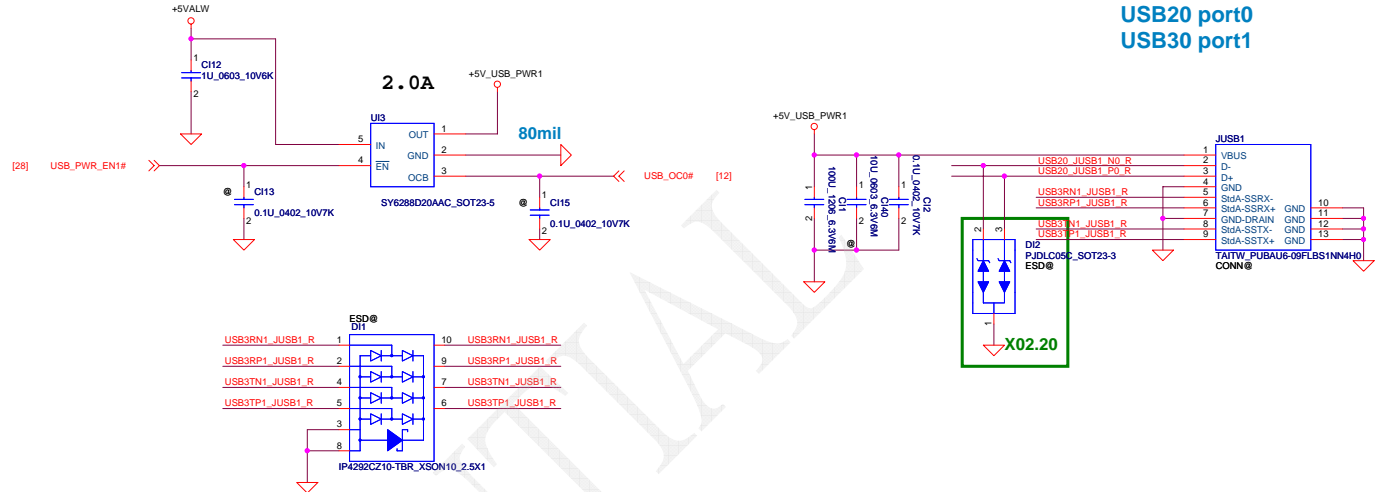
Trace width for SPK-L+/SPK-L-/SPK-R+/SPK-R-  
Speaker 4 ohm : 40mil  
Speaker 8 ohm : 20mil

iPhone and Nokia type Combo Jack

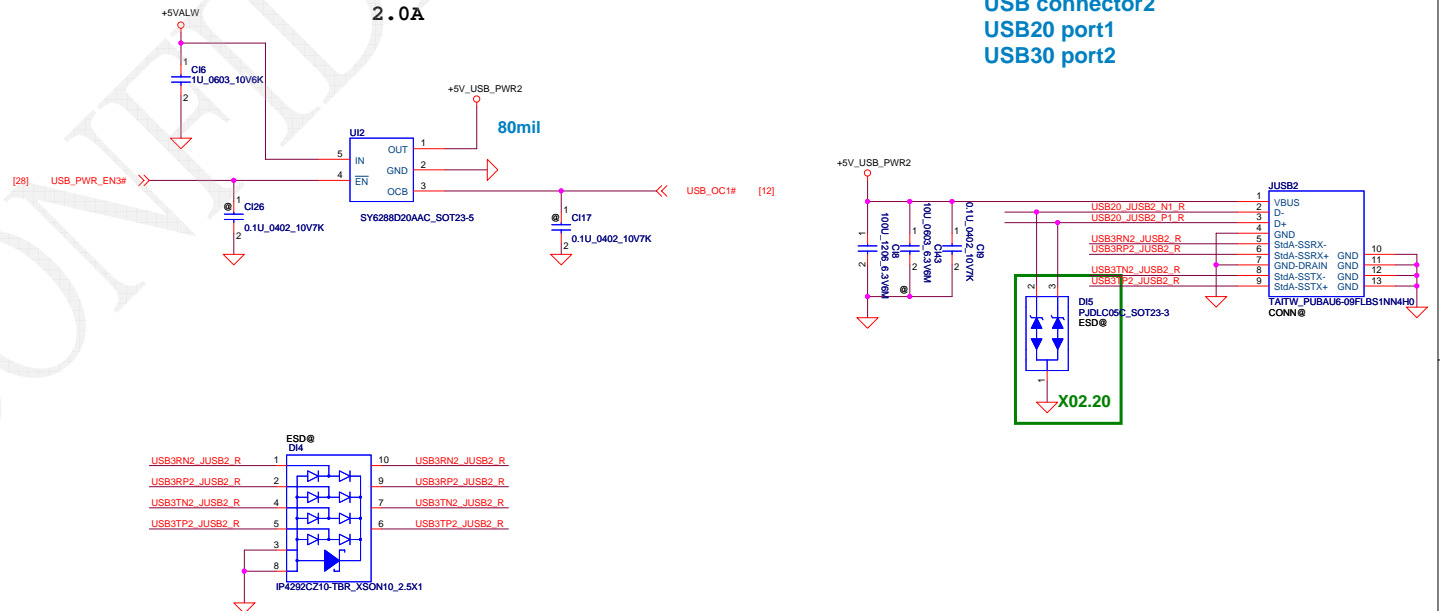


|                         |                    |                 |            |                              |  |
|-------------------------|--------------------|-----------------|------------|------------------------------|--|
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|                         |                    |                 |            | SCHEAMTICS.MB AB072          |  |
|                         |                    |                 |            | Rev A                        |  |
|                         |                    |                 |            | Date: Monday, April 07, 2014 |  |
|                         |                    |                 |            | Sheet 23 of 54               |  |





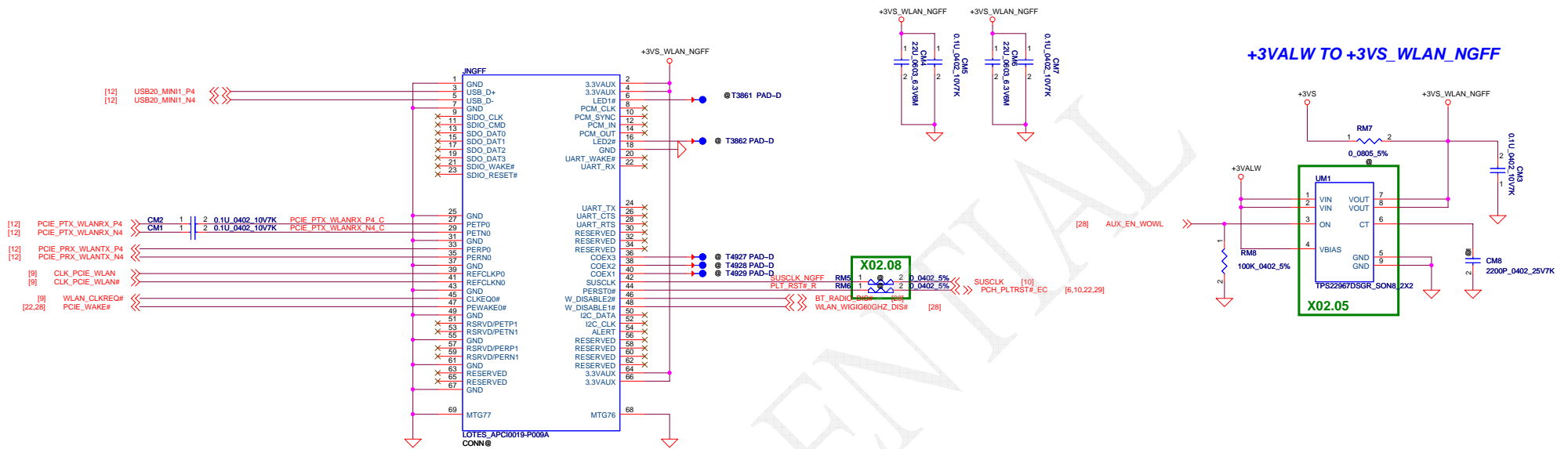
USB connector1  
USB20 port0  
USB30 port1



USB connector2  
USB20 port1  
USB30 port2

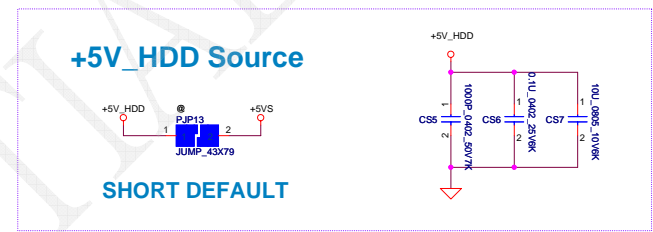
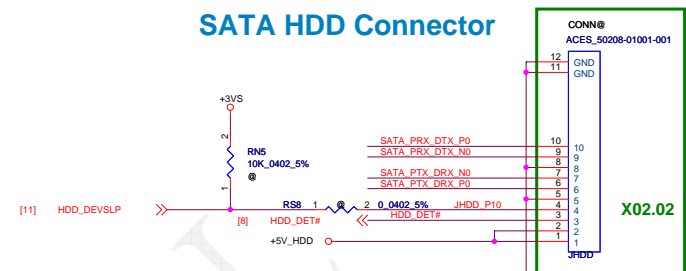
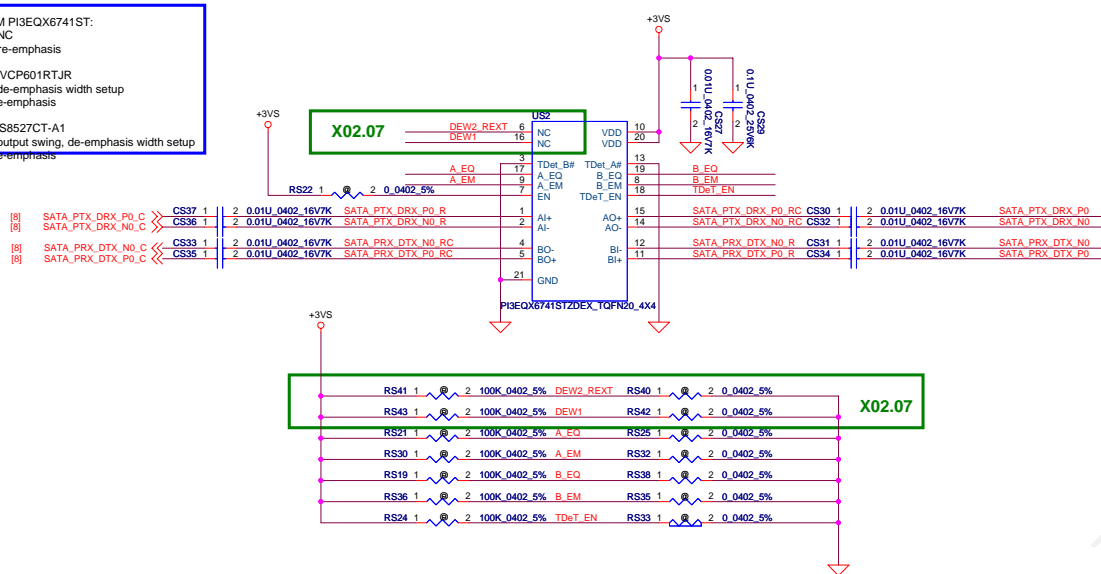


closed to pin 2, 4      closed to pin 64, 66



|   |            |                    |            |                          |                        |
|---|------------|--------------------|------------|--------------------------|------------------------|
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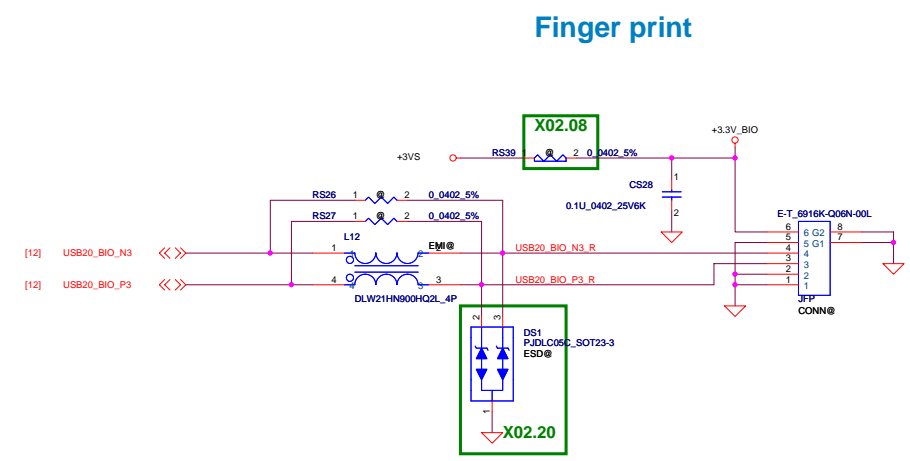
PERICOM PI3EQX6741ST:  
Pin6/16, NC  
Pin8/9, Pre-emphasis  
  
TI SN75LVCP601RTJR  
Pin6/16, de-emphasis width setup  
Pin8/9, de-emphasis  
  
Parade PS8527CT-A1  
Pin6/16, output swing, de-emphasis width setup  
Pin8/9, de-emphasis

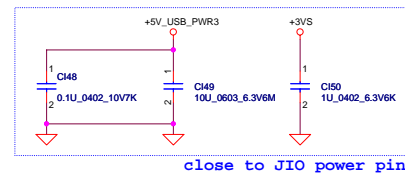
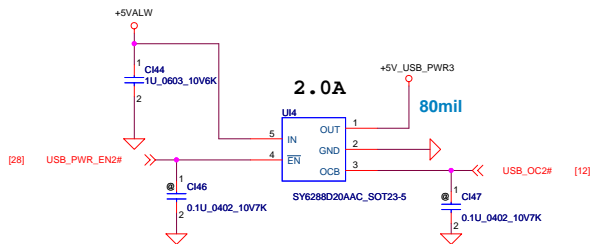


|                      |  | DEW2      | B_EM      | A_EM      | Tdet_A | DEW1     | A_EQ      | Tdet_EN   | B_EQ      |
|----------------------|--|-----------|-----------|-----------|--------|----------|-----------|-----------|-----------|
|                      |  | PIN6      | PIN8      | PIN9      | PIN13  | PIN16    | PIN17     | PIN18     | PIN19     |
| Pericom PI3EQX6741ST |  | NC        | PD (RS35) | NC (IP0)  | PD     | NC       | NC        | PH (RS24) | PD (RS38) |
| TI SN75LVCP601       |  | NC (IP0)  | PD (RS35) | PD (RS32) | PD     | NC (IP0) | PD (RS25) | PD (RS33) | NC        |
| Parade PS8527C       |  | PD (RS40) | PD (RS35) | PH (RS30) | PD     | NC       | PD (RS25) | PD (RS33) | NC        |

|      |         |  | A_EQ  | B_EQ  |                                      | A_EM  | B_EM  |
|------|---------|--|---|---|--------------------------------------|---|---|
| Main | Pericom | 0<br>NC<br>1   | 3dB<br>6dB<br>9dB   | 3dB<br>6dB<br>9dB   | 0<br>NC<br>1                         | 0dB<br>1.5dB<br>1.5dB   | 0dB<br>1.5dB<br>1.5dB   |
| 2nd  | TI      | 0<br>NC<br>1   | 7dB<br>0dB<br>14dB  | 7dB<br>0dB<br>14dB  | 0<br>NC<br>1                         | 0dB<br>-6dB<br>-3dB   | 0dB<br>-6dB<br>-3dB   |
| 3rd  | Parade  | EQ2<br>EQ1<br>(M = VDD/2)<br>0 M<br>0 0<br>0 1<br>M M<br>M 0<br>M 1<br>1 M<br>1 0<br>1 1 | 2.4dB<br>7.4dB<br>14.4dB<br>12.2dB<br>9.4dB<br>13.3dB<br>6.2dB<br>11.2dB<br>5dB | 2.4dB<br>7.4dB<br>14.4dB<br>12.2dB<br>9.4dB<br>13.3dB<br>6.2dB<br>11.2dB<br>5dB | 0<br>M<br>1<br>M<br>1<br>0<br>1<br>1 | 0dB<br>-3.5dB<br>-1.5dB<br>-3.5dB<br>-1.5dB<br>-3.5dB<br>-1.5dB<br>-3.5dB<br>-1.5dB | 0dB<br>-3.5dB<br>-1.5dB<br>-3.5dB<br>-1.5dB<br>-3.5dB<br>-1.5dB<br>-3.5dB<br>-1.5dB |

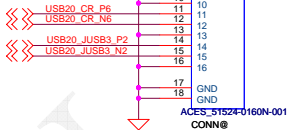
\* red color is current setting





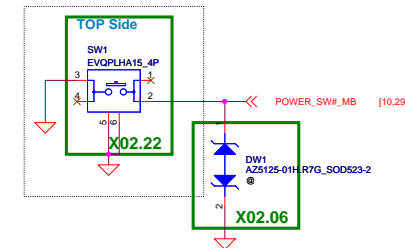
close to J10 power pin

[12] USB20\_CR\_P6  
[12] USB20\_CR\_N6  
[12] USB20\_JUSB3\_P2  
[12] USB20\_JUSB3\_N2

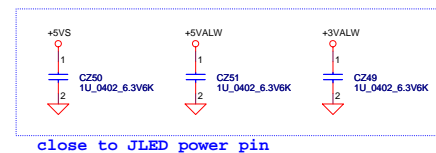
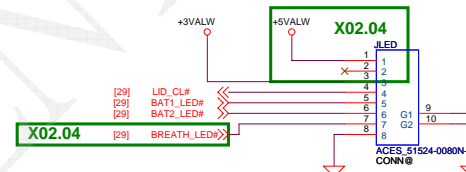


## IO to MB CONN

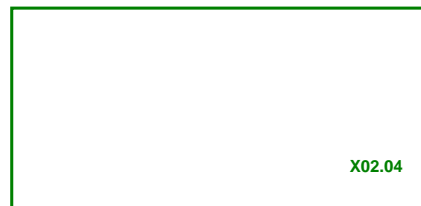
## ON/OFF switch



## LED/B TO M/B

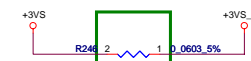
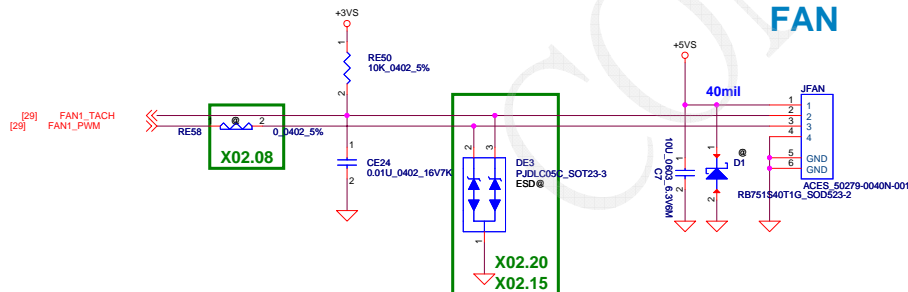


close to JLED power pin

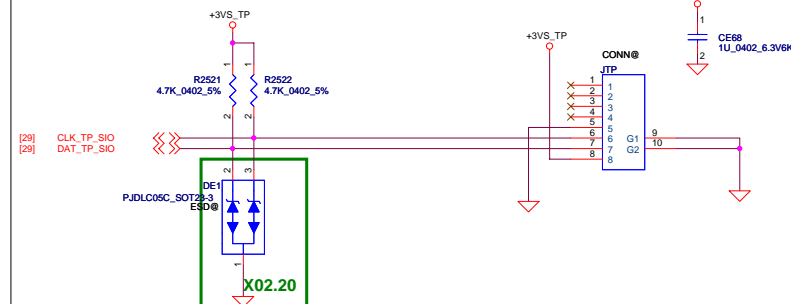


X02.04

## FAN



## Touch pad

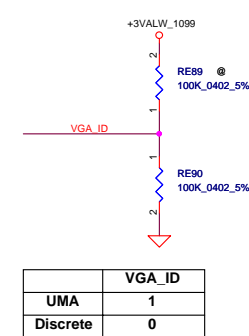
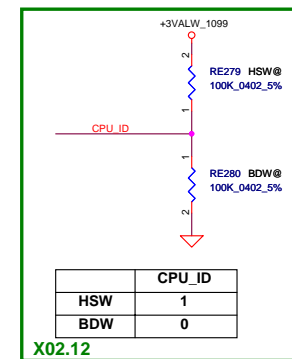
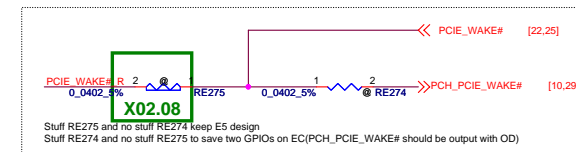
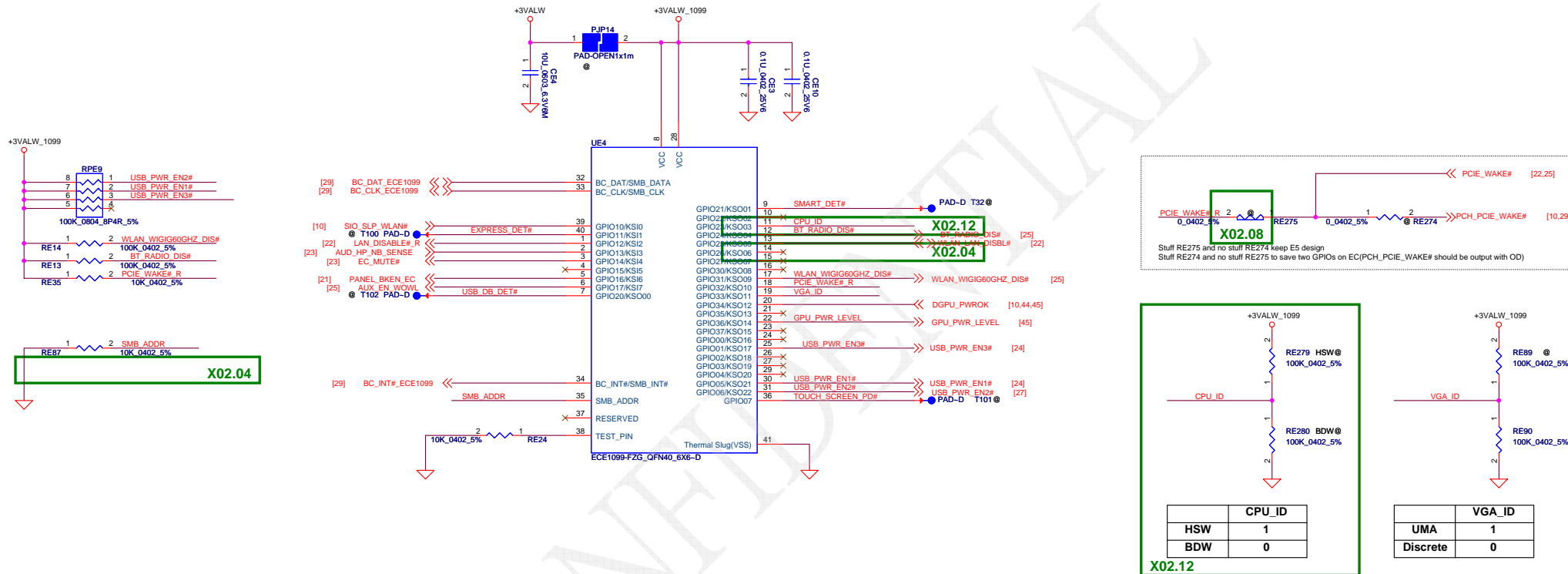


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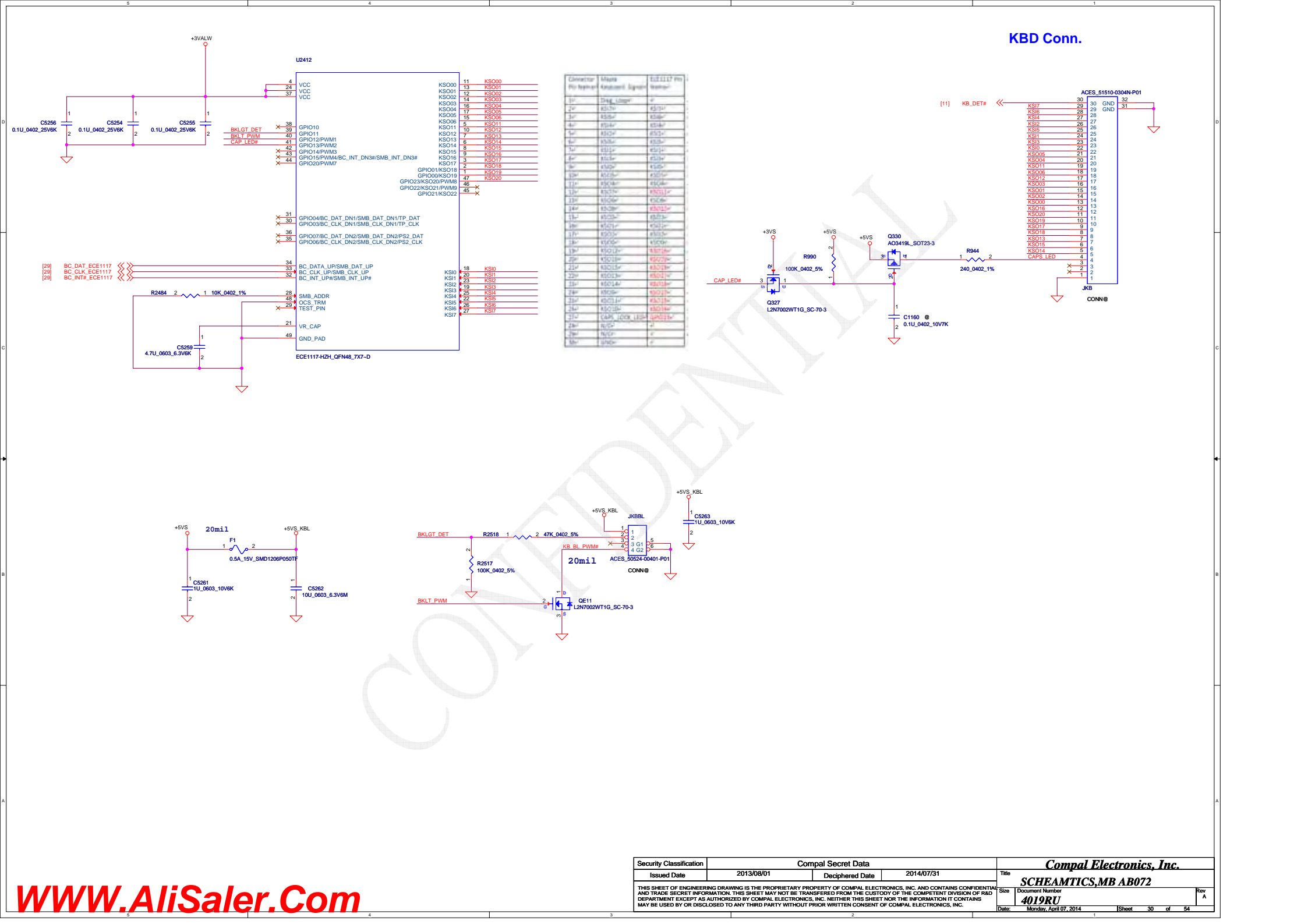
Monday, April 07, 2014 27 of 54



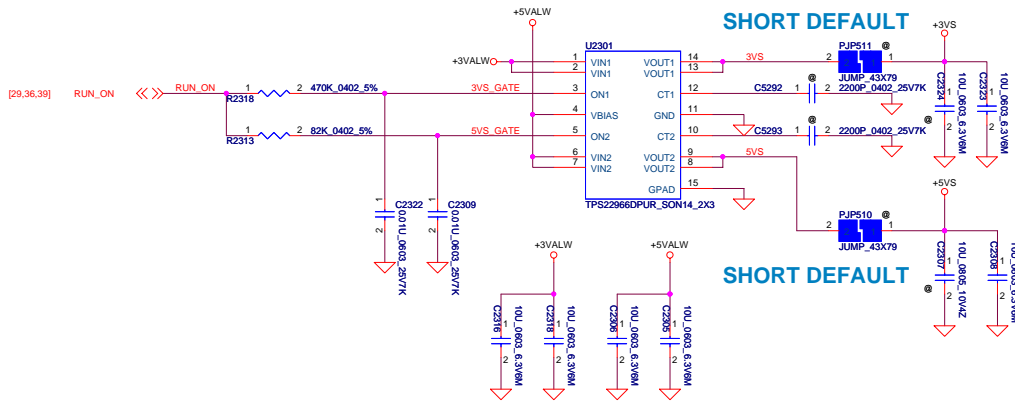
|     | CPU_ID |
|-----|--------|
| HSW | 1      |
| BDW | 0      |

|          | VGA_ID |
|----------|--------|
| UMA      | 1      |
| Discrete | 0      |

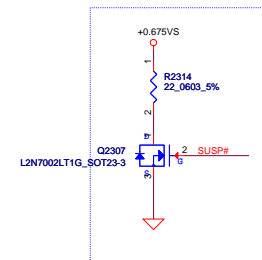
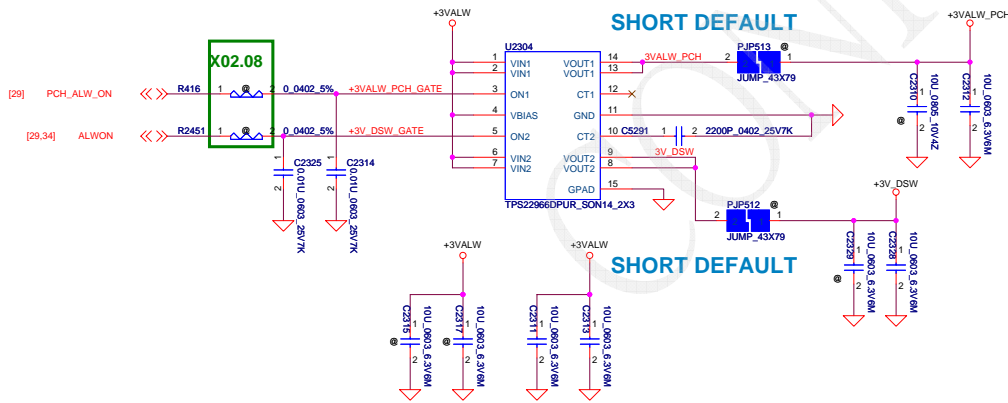




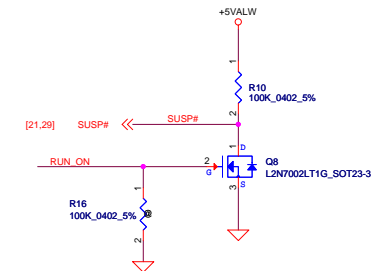
## +5VS and +3VS switch



## +3VALW\_PCH switch

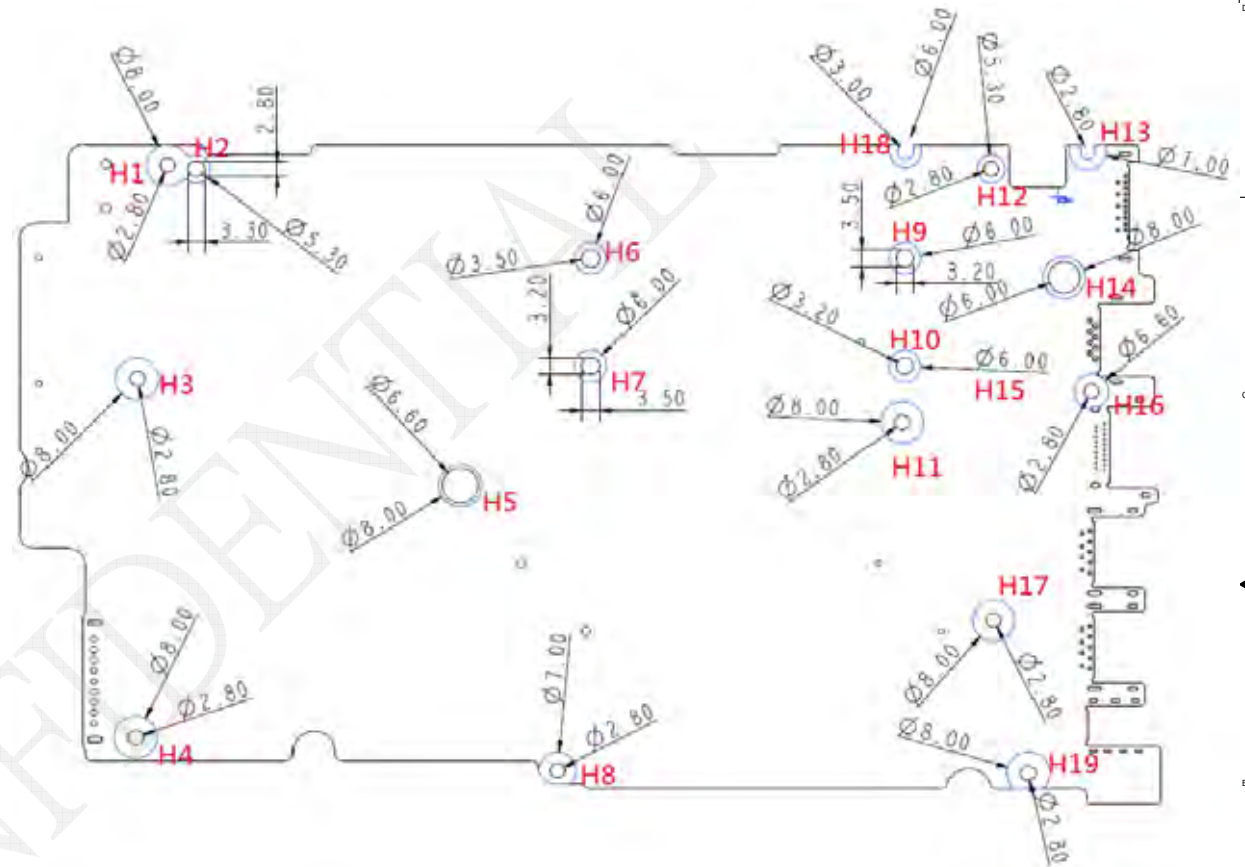
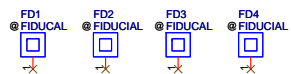
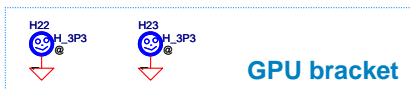
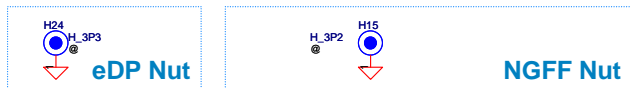
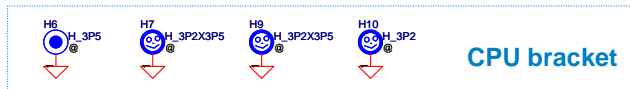
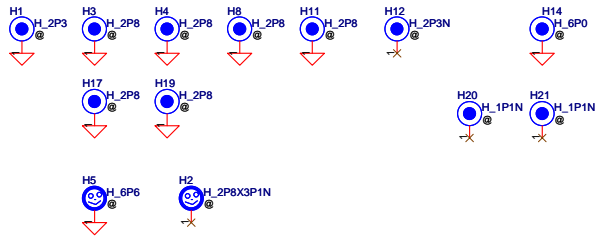


For Intel S3 Power Reduction



|   |            |                    |            |                 |                        |
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|   |            |                    |            | Sheet           | 31 of 54               |

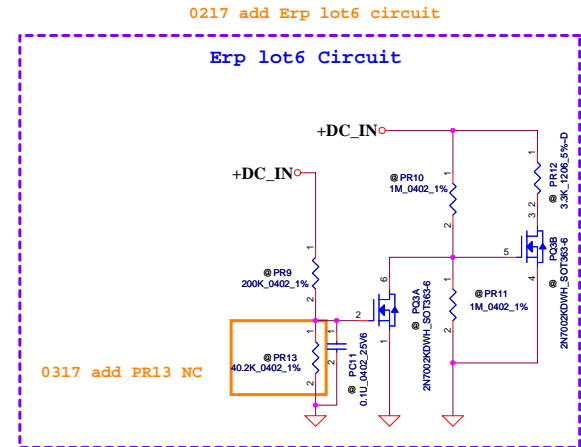
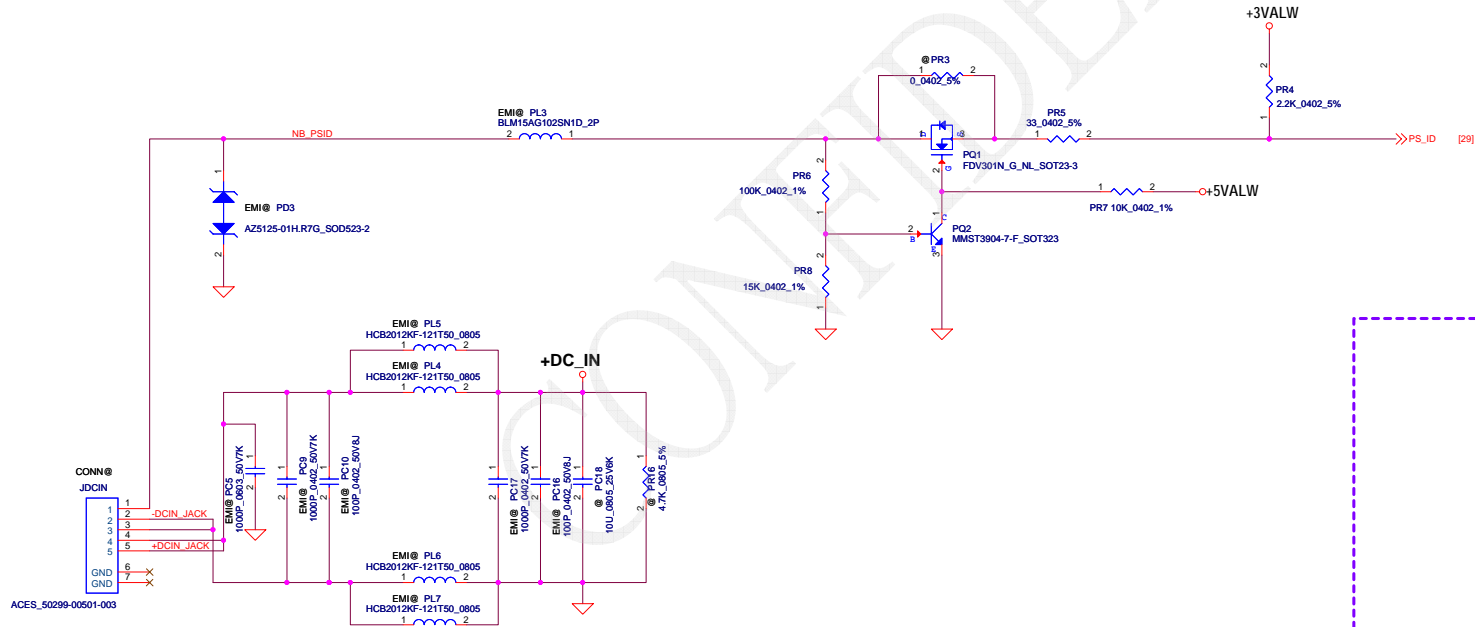
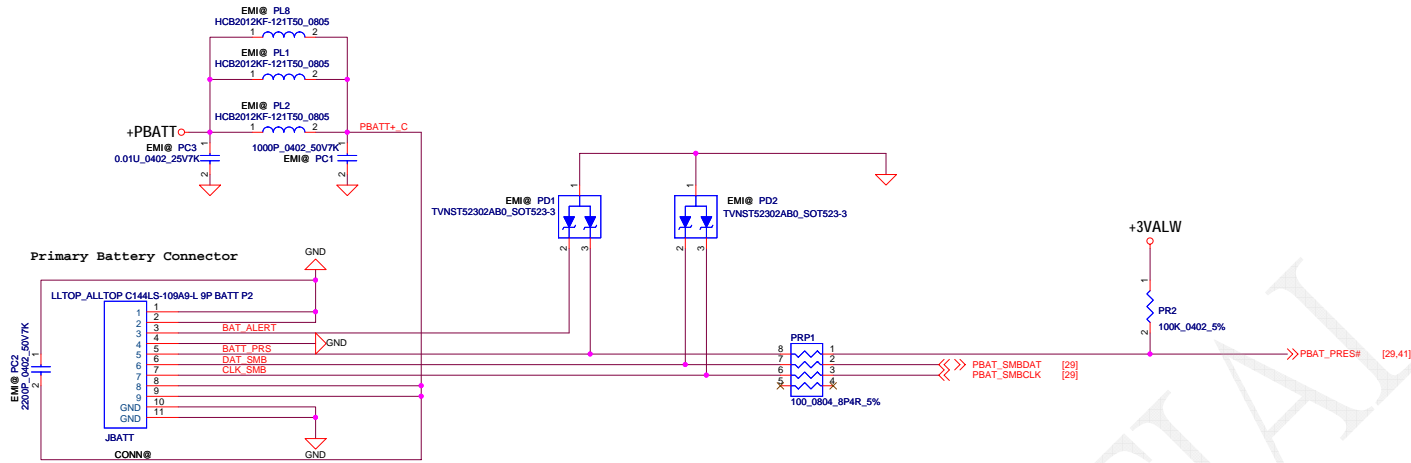
## Screw Hole



|   |                    |                 |            |                          |                        |
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SMART  
Battery:  
01.GND1  
02.GND2  
03.BAT\_ALERT  
04.SYS\_PRES  
05.BATT\_PRS  
06.DAT\_SMB  
07.CLK\_SMB  
08.BATT1+  
09.BATT2+





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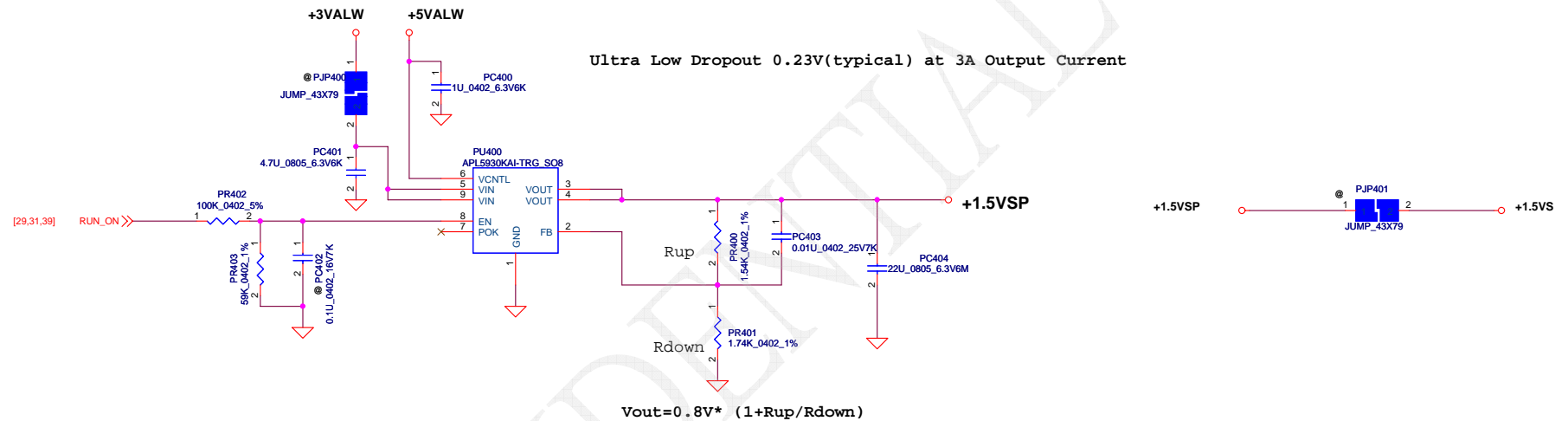


[0823] change DP to VGA solution, delet this design

|   |            |                    |            |                          |                        |
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# Module model information

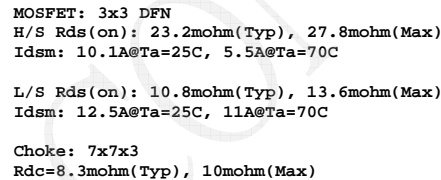
APL5930\_V1.mdd



1.5VS  
TDC 0.014A  
Peak Current 0.2A  
OCP current 5.7A

|   |                    |                 |                          |                              |
|---|--------------------|-----------------|--------------------------|------------------------------|
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|   |                    |                 |                          | Rev A                        |

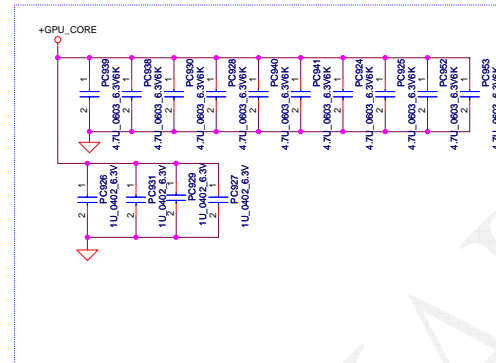
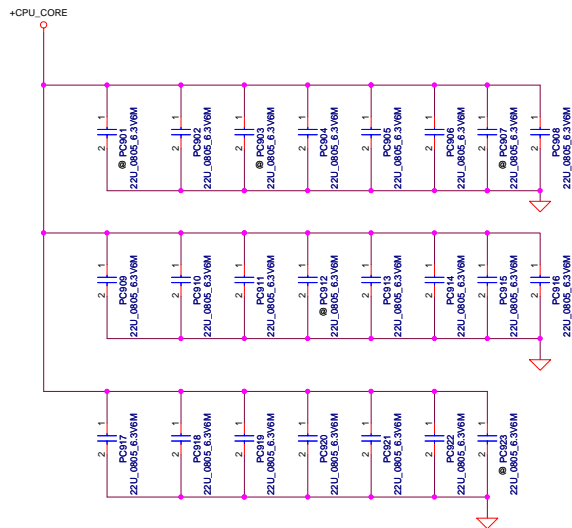
|                |                  |
|----------------|------------------|
| RT8207M_V1.mdd | For Single layer |
| RT8207M_V2.mdd | For Dual layer   |



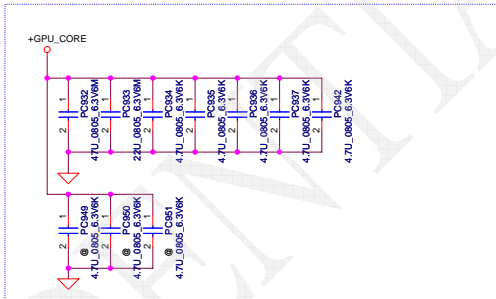
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nVidia GB2B-64 package  
Under GPU  
4.7uF 0603 \* 10  
1uF 0402 \* 4

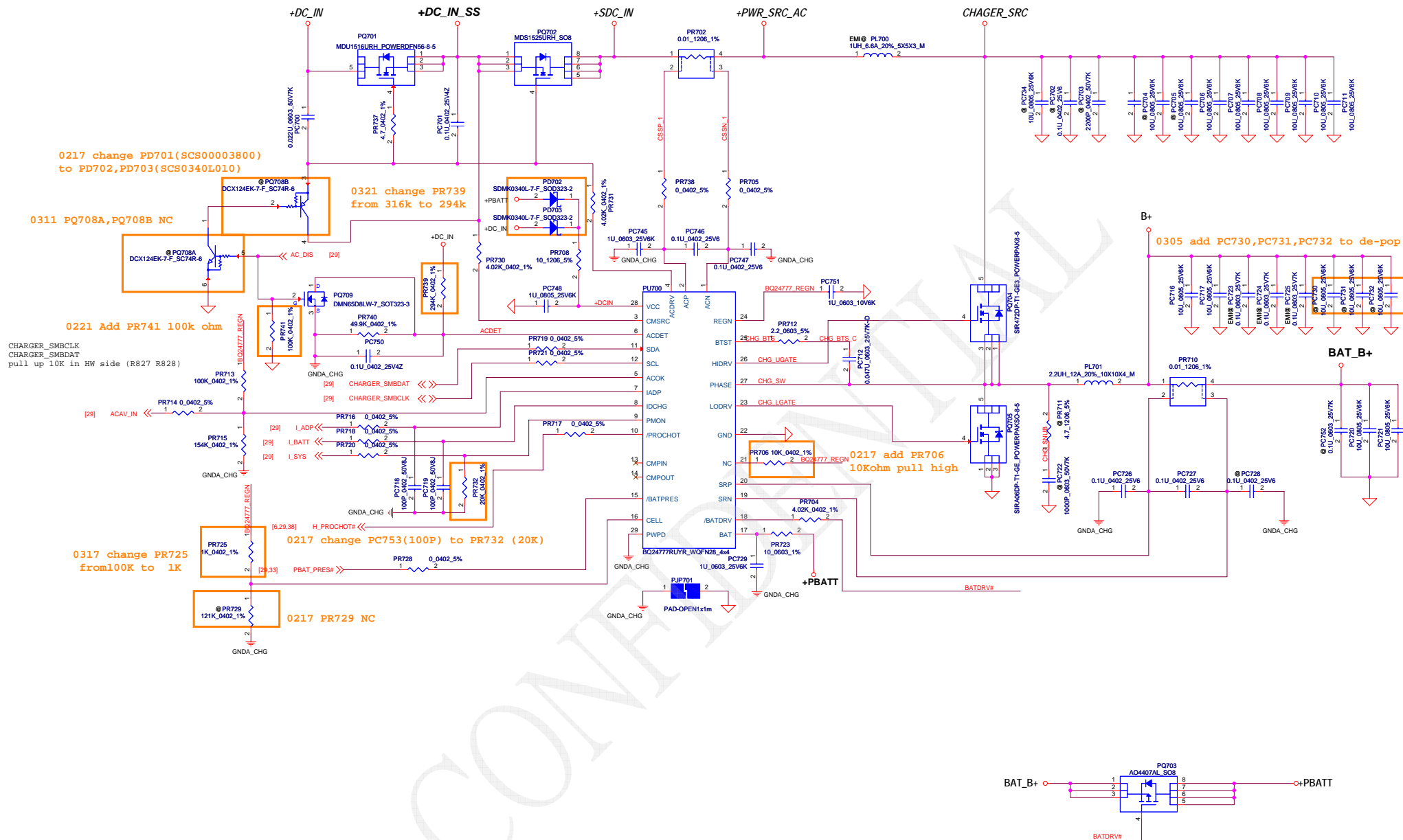


nVidia GB2B-64 package  
Near GPU  
47uF 0805 \*1  
22uF 0805 \*1  
4.7uF 0805 \*5

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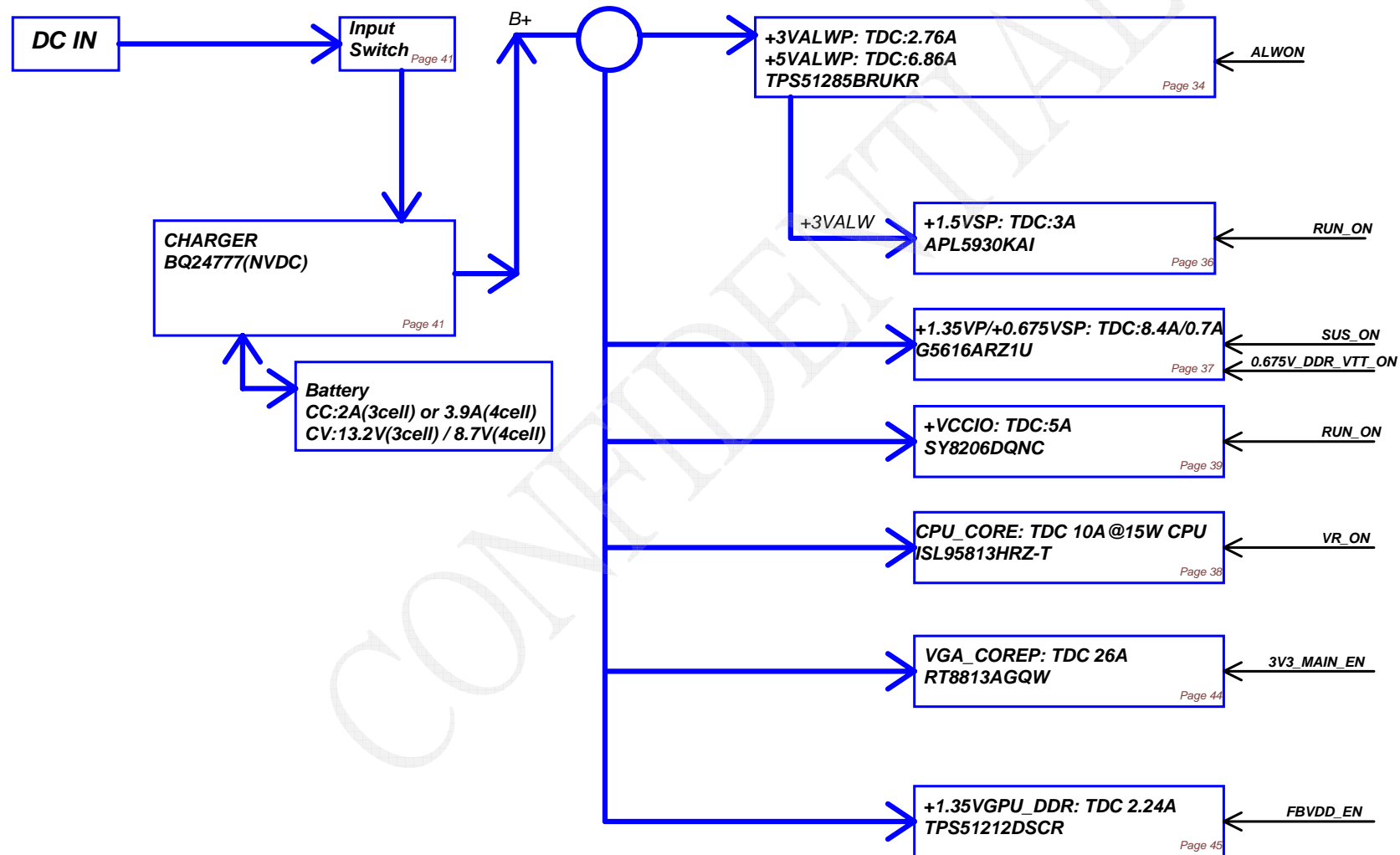




DELTA CONFIDENTIAL/PROPRIETARY

|   |            |                    |            |                     |                 |
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# Power block



|   |            |                    |            |                          |                        |
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|   |            |                    |            | Sheet                    | 42 of 54               |

$V_{boot} = V_{vref} * R_{ref2} / (R_{ref1} + R_{ref2} + R_{boot})$   
 $R_t = R_{refadj} // (R_{boot} + R_{ref2})$   
 $V_{min} = V_{vref} * [R_{ref2} / (R_{ref2} + R_{boot})] * [R_t / (R_{ref1} + R_t)]$   
 $V_{max} = V_{vref} * R_{ref2} / [(R_{ref1} // R_{refadj}) + R_{boot} + R_{ref2}]$   
 $V_{out} = V_{min} + N * V_{step}$   
 $V_{step} = (V_{max} - V_{min}) / N_{max}$

#### PWM-VID Spec and component Values

| PWM-VID Spec       | Config A | Config B | Config C |
|--------------------|----------|----------|----------|
| Vmin               | 0.6V     | 0.6V     | 0.65V    |
| Vmax               | 1.2V     | 1.2V     | 1.15V    |
| Vboot              | 0.875V   | 0.9V     | 0.9V     |
| Voltage step       | 6.25mV   | 6.25mV   | 25mV     |
| N of Voltage level | 96       | 96       | 20       |
| Rrefadj            | PR604    | 39K      | 20K      |
| Rref1              | PR602    | 39K      | 20K      |
| Rboot              | PR603    | 1.5K     | 2K       |
| Rref2=PR607+PR610  | PR607    | 30K      | 18K      |
|                    | PR610    | 1.5K     | 0        |
| C                  | PC607    | 1.5nf    | 2.7nf    |

H-side MOS:MDU1516URH  
 Rds(on):  
 11.7mohm@Vgs=4.5V  
 Id :18.6A@Ta=25 degC

L-side MOS:MDU1511RH  
 Rds(on):  
 2.7mohm@Vgs=4.5V  
 Id :36.1A@Ta=25 degC

Different VGA Chip (different EDP-Peak Current) need select different solution

| VGA Chip                     | N15S-GM     |
|------------------------------|-------------|
| OpenVReg Configurations      | Config B    |
| Rated TDP Power at Tj=102C   | 18W         |
| Boosted GPU Total at Tj=102C | 20W         |
| EDP-Continuous at Tj=102C    | 22A         |
| EDP-Peak at Tj=102C          | 48.11 A     |
| Istep max (Evaluation)       | 29.22 A     |
| OCF Setting Current          | 66A         |
| Rocset                       | 13K         |
| Recommendation               | 2phase 1H1L |
| Polymer Cap (330uF)          | 9mohm * 3   |
| Or OSCON (390uF)             | NULL        |

PWM VID and Output voltage control  
 1.Boot mode  
 2.Standby mode (don't support)  
 3.Normal mode

| Operation phase Number | PSI Voltage setting |
|------------------------|---------------------|
| 1 phase with DEM       | 0V to 0.8V          |
| 1 phase with CCM       | 1.2V to 1.8V        |
| Active phase with CCM  | 2.4V to 5.5V        |

PSI Pull high on HW side

Pull high on HW side

Reserve Location

0217 PC604 change from pop to de-pop  
 PC627 change from de-pop to pop

+VGA\_CORE  
 EDP-Continuous 22A  
 EDP-Peak 48.11A  
 OCP min 66A

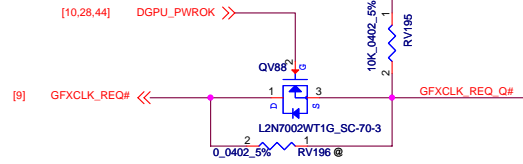
- VSNS Soft-Start time (Internal) is 0.7ms (PC616 un-pop)  
 $T_{ss} = (C_{ss} * V_{refin}) / I_{ss} + 2.3ms$   
 $= 0.01uF * 0.9V / 5uA + 2.3ms = 4.1ms$  (PC616 pop)
- Switching frequency setting:  
 $F_{sw} = (V_{in} - 0.5) / (2 * V_{in} * R_{ton} * 3.2p) = 304.89KHz$



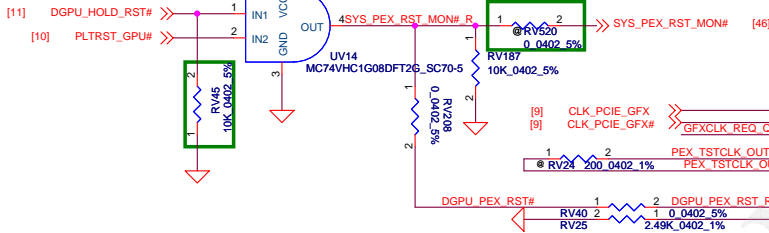
[12] PEG\_CTX\_GRX\_P[0..3] >> PEG\_CTX\_GRX\_P[0..3]  
 [12] PEG\_CTX\_GRX\_N[0..3] >> PEG\_CTX\_GRX\_N[0..3]  
 [12] PEG\_CRX\_GTX\_P[0..3] << PEG\_CRX\_GTX\_P[0..3]  
 [12] PEG\_CRX\_GTX\_N[0..3] << PEG\_CRX\_GTX\_N[0..3]

|                |       |   |   |       |      |       |                  |
|----------------|-------|---|---|-------|------|-------|------------------|
| PEG_CRX_GTX_P0 | CV188 | 2 | 1 | 0.22U | 0402 | 16V7K | PEG_CRX_GTX_C_P0 |
| PEG_CRX_GTX_N0 | CV189 | 2 | 1 | 0.22U | 0402 | 16V7K | PEG_CRX_GTX_C_N0 |
| PEG_CRX_GTX_P1 | CV190 | 2 | 1 | 0.22U | 0402 | 16V7K | PEG_CRX_GTX_C_P1 |
| PEG_CRX_GTX_N1 | CV191 | 2 | 1 | 0.22U | 0402 | 16V7K | PEG_CRX_GTX_C_N1 |
| PEG_CRX_GTX_P2 | CV192 | 2 | 1 | 0.22U | 0402 | 16V7K | PEG_CRX_GTX_C_P2 |
| PEG_CRX_GTX_N2 | CV193 | 2 | 1 | 0.22U | 0402 | 16V7K | PEG_CRX_GTX_C_N2 |
| PEG_CRX_GTX_P3 | CV194 | 2 | 1 | 0.22U | 0402 | 16V7K | PEG_CRX_GTX_C_P3 |
| PEG_CRX_GTX_N3 | CV195 | 2 | 1 | 0.22U | 0402 | 16V7K | PEG_CRX_GTX_C_N3 |

+3.3V\_RUN GFX



+3.3V\_RUN GFX



[28] GPU\_PWR\_LEVEL >> DV3 >> GPU\_HOT#

| GPU_PWR_LEVEL |                  |
|---------------|------------------|
| LOW           | Low Performance  |
| HIGH          | High Performance |

PEG\_CTX\_GRX\_P0 AG6  
 PEG\_CTX\_GRX\_N0 AG7  
 PEG\_CTX\_GRX\_P1 AF7  
 PEG\_CTX\_GRX\_N1 AE7  
 PEG\_CTX\_GRX\_P2 AE9  
 PEG\_CTX\_GRX\_N2 AF9  
 PEG\_CTX\_GRX\_P3 AG9  
 PEG\_CTX\_GRX\_N3 AG10

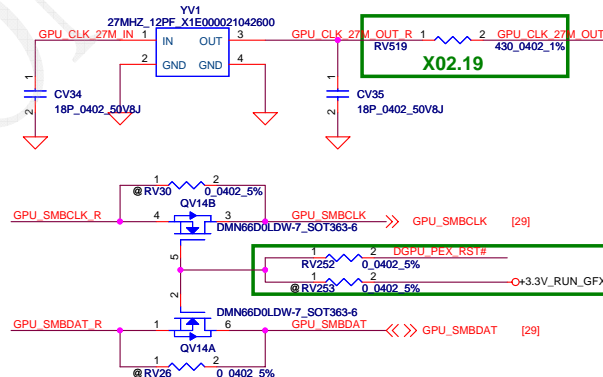
AF10 NC  
 AE12 NC  
 AF12 NC  
 AG12 NC  
 AG13 NC  
 AF13 NC  
 AE13 NC  
 AE15 NC  
 AF15 NC  
 AG16 NC  
 AF16 NC  
 AE16 NC  
 AG17 NC  
 AF18 NC  
 AG18 NC  
 AG19 NC  
 AF19 NC  
 AE19 NC  
 AE21 NC  
 AF21 NC  
 AG21 NC  
 AG22 NC

PEG\_CRX\_GTX\_C\_P0 AC9  
 PEG\_CRX\_GTX\_C\_N0 AB9  
 PEG\_CRX\_GTX\_C\_P1 AB10  
 PEG\_CRX\_GTX\_C\_N1 AC10  
 PEG\_CRX\_GTX\_C\_P2 AD11  
 PEG\_CRX\_GTX\_C\_N2 AC11  
 PEG\_CRX\_GTX\_C\_P3 AC12  
 PEG\_CRX\_GTX\_C\_N3 AB12

AB13 NC  
 AC13 NC  
 AD14 NC  
 AC14 NC  
 AC15 NC  
 AB15 NC  
 AB16 NC  
 AC16 NC  
 AD17 NC  
 AC17 NC  
 AB18 NC  
 AB19 NC  
 AC19 NC  
 AD20 NC  
 AC20 NC  
 AC21 NC  
 AB21 NC  
 AD23 NC  
 AE23 NC  
 AF24 NC  
 AG24 NC  
 AG25 NC

AE8 PEX\_REFCLK  
 AD8 PEX\_REFCLK\_N  
 AC6 PEX\_CLKREQ\_N  
 AF22 PEX\_TSTCLK\_OUT  
 AE22 PEX\_TSTCLK\_OUT\_N  
 AC7 PEX\_RST\_N  
 AF25 PEX\_THERMP

GM108-ES-S-A1\_FCBGA595



### SP\_PLLVDD and VID\_PLLVDD Power rail Filtering Combined

| Capacitor Type                  | Population |
|---------------------------------|------------|
| 0.1uF 0402                      | 1 per ball |
| 4.7uF 0603                      | 1          |
| 22uF 0805                       | 1          |
| Bead 180 ohm (ESR=0.2 ohm) 0603 | 1          |

### PLLVDD Filtering

| Capacitor Type                  | Population |
|---------------------------------|------------|
| 0.1uF 0402                      | 1          |
| 22uF 0805                       | 1          |
| Bead 30 ohm (ESR=0.05 ohm) 0402 | 1          |

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Security Classification

Compal Secret Data

Issued Date

2013/07/25

Deciphered Date

2014/07/24

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Title

SCHEMATICS, MB AB072

Rev

4019RU

Rev

Date: Monday, April 07, 2014

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## I2CS Slave Address

| SMBUS_ALT_ADDR | Description           |
|----------------|-----------------------|
| 0              | 0x9E(Default)         |
| 1              | 0x9C(Multi-GPU usage) |

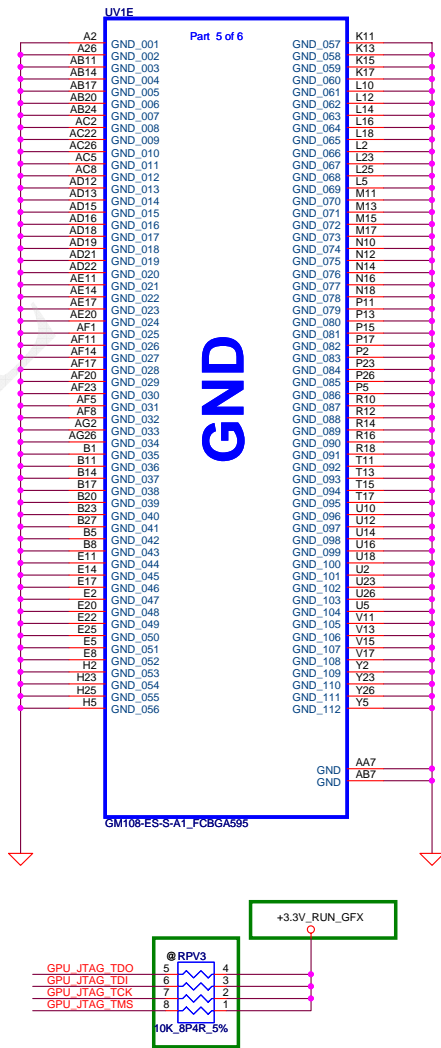
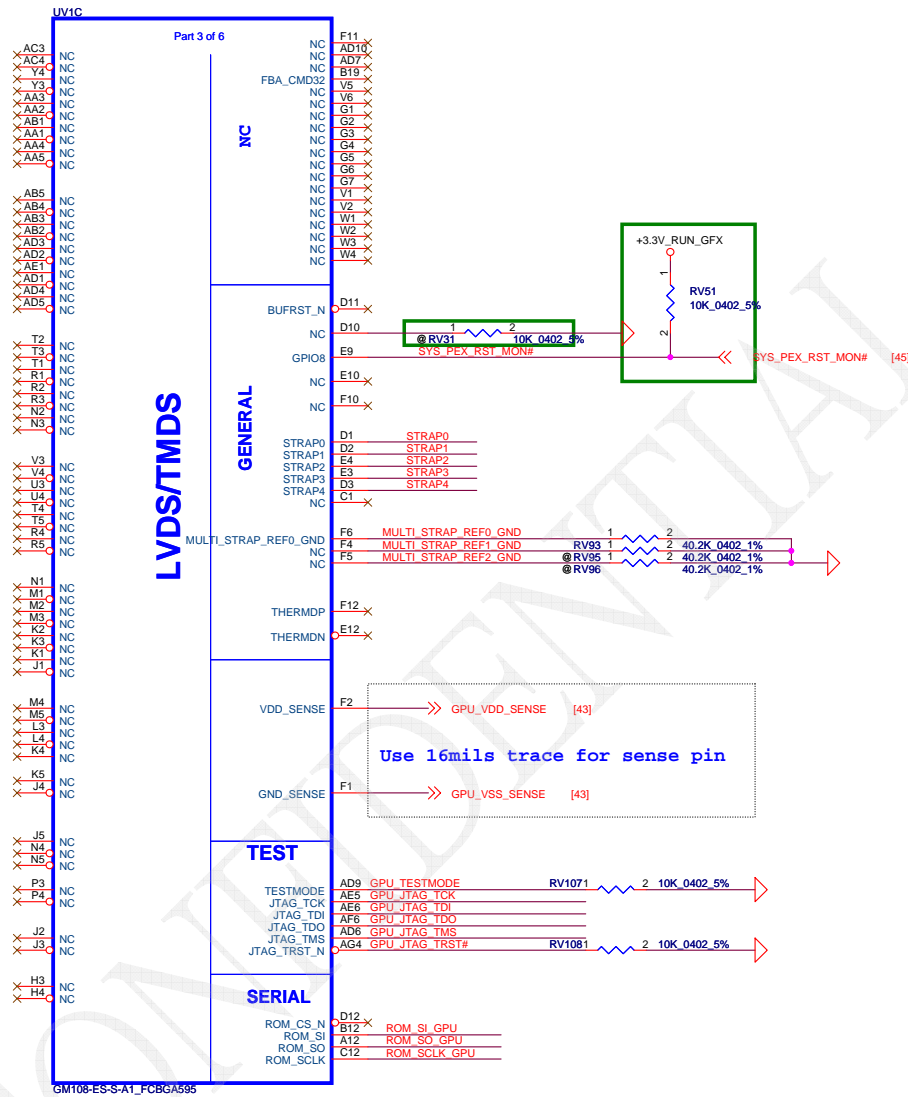
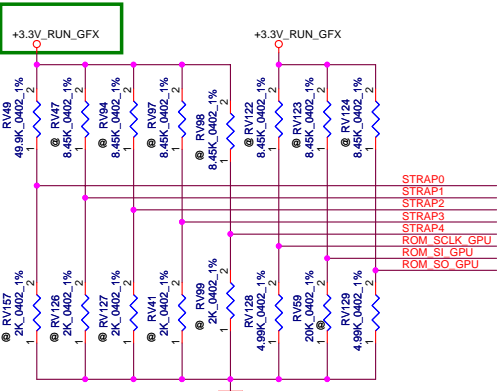
### VGA\_DEVICE Setting

| VGA_DEVICE | Description   |
|------------|---|
| 0          | Non-Primary 3D Acceleration Device(Class Code 302h) |
| 1          | Primary Display or VGA Device(Class Code 300h)      |

### Resistance Mapping to Hex Values

| Resistor Value | Pull-up to VDD33 | Pull-down to GND |
|----------------|------------------|------------------|
| 4.99K          | 1000             | 0000             |
| 10K            | 1001             | 0001             |
| 15K            | 1010             | 0010             |
| 20K            | 1011             | 0011             |
| 24.9K          | 1100             | 0100             |
| 30.1K          | 1101             | 0101             |
| 34.8K          | 1110             | 0110             |
| 45.3K          | 1111             | 0111             |

Decive ID change to 0x1056



| Strap Pin Name                       | Logical Strapping Bit 3  | Logical Strapping Bit 2 | Logical Strapping Bit 1  | Logical Strapping Bit 0 | Note                                |
|--------------------------------------|--|-------------------------|--------------------------|-------------------------|-------------------------------------|
| ROM_SCLK                             | SOR3_EXPOSED->0  | SOR2_EXPOSED->0         | SOR1_EXPOSED->0          | SOR0_EXPOSED->0         | ROM_SCLK pull-down 4.99k to GND     |
| ROM_SI                               | RAM_CFG[3]   | RAM_CFG[2]              | RAM_CFG[1]               | RAM_CFG[0]              | ROM_SI pull-down 20k to GND         |
| ROM_SO                               | DEVID_SEL->0(default)  | PCIE_CFG->0(default)    | SMB_ALT_ADDR->0(default) | VGA_DEVICE->0           | ROM_SO pull-down 4.99k to GND       |
| STRAP0                               | Keep pull up to 3V3_AON and pull-down to GND footprint and stuff 50k ohm pull up |                         |                          |                         | STRAP0 pull up 50k to +3.3V_GFX_AON |
| STRAP1<br>STRAP2<br>STRAP3<br>STRAP4 | Reserve  |                         |                          |                         |                                     |

| VENDER  | STRAP | Part Number         | Note(ROM_Sl) |
|---------|-------|---------------------|--------------|
| Hynix   | 0x3   | H5TC4G63AFR-11C     | 20k PD       |
| Micron  | 0x4   | MT41J256M16HA-093GE | 24.9k PD     |
| Samsung | 0x5   | K4W4G1646D-BC1A     | 30.1k PD     |

Base on RVL RVL-06891-001\_v03\_secured.pdf

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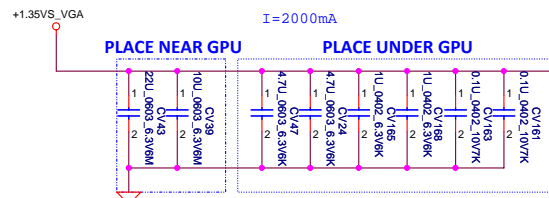
**Compal Electronics, Inc.**

Title **SCHEAMTICS,MB AB072**

|                      |                                  |                              |                |
|----------------------|----------------------------------|------------------------------|----------------|
| ENGIN<br>F R&D<br>IS | Document Number<br><b>4019RU</b> | Date: Monday, April 07, 2014 | Sheet 46 of 54 |
|----------------------|----------------------------------|------------------------------|----------------|

| For the latest configuration  |                           |                 |                   |
|---|---------------------------|-----------------|-------------------|
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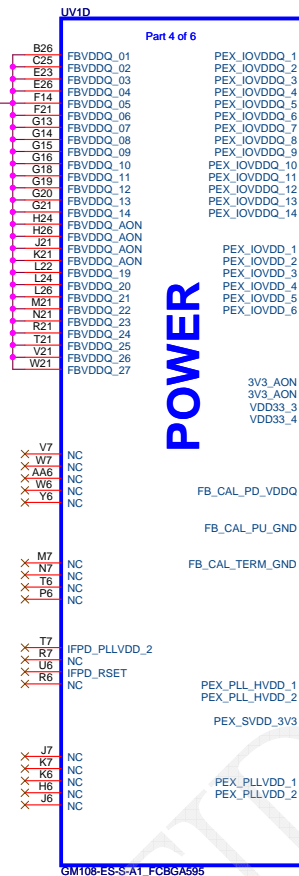
**WWW.AliSaler.Com**



DDR3 CPU side FBVDDQ/FBVDDQ2  
Combined Decoupling

| Capacitor Type | Population |
|----------------|------------|
| 0.1uF 0402     | 2          |
| 1.0uF 0603     | 2          |
| 4.7uF 0603     | 2          |
| 10uF 0805      | 1          |
| 22uF 0805      | 1          |

| Power Supply Rail  |             | N15S-GM      | N15S-GT      |
|--------------------|-------------|--------------|--------------|
|                    | (V)         | (A)          | (A)          |
| GPU_Core           | -           | 26           | 31           |
| GPU_FBIO           | 1.5/1.35    | TBD          | TBD          |
| PEX_IOVDD/Q        | 1.05        | 0.765        | 0.765        |
| PEX_PLLVDD         | 1.05        | 0.130        | 0.130        |
| FBA_PLL_AVDD       | 1.05        | 0.062        | 0.062        |
| FBA_DLL_AVDD       | 1.05        | 0.032        | 0.032        |
| PLL_VDD            | 1.05        | 0.058        | 0.058        |
| SP_PLLVDD          | 1.05        | 0.030        | 0.030        |
| <b>1.05V Total</b> | <b>1.05</b> | <b>1.060</b> | <b>1.060</b> |
| VDD33+3V3AON       | 3.3         | 0.036        | 0.036        |
| PEX_SVDD_3V3       | 3.3         | 0.167        | 0.167        |
| PEX_PLL_HVDD       | 3.3         | 0.022        | 0.022        |
| <b>3.3V Total</b>  | <b>3.3</b>  | <b>0.225</b> | <b>0.025</b> |



POWER

PEX\_PLLVDD Decoupling

| Capacitor Type | Population |
|----------------|------------|
| 0.1uF 0402     | 1          |
| 1uF 0603       | 1          |
| 4.7uF 0805     | 1          |

PEX\_SVDD/PEX\_PLL\_HVDD Decoupling

| Capacitor Type | Population |
|----------------|------------|
| 0.1uF 0402     | 1          |
| 4.7uF 0603     | 2          |

3V3\_MAIN Decoupling

| Capacitor Type | Population |
|----------------|------------|
| 0.1uF 0402     | 2          |
| 1uF 0603       | 1          |
| 4.7uF 0603     | 1          |

3V3\_AON Decoupling

| Capacitor Type | Population |
|----------------|------------|
| 0.1uF 0402     | 1          |
| 1uF 0603       | 1          |
| 4.7uF 0603     | 1          |

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|   |                    |                 |            | 4019RU                       | A              |
|   |                    |                 |            | Date: Monday, April 07, 2014 | Sheet 47 of 54 |

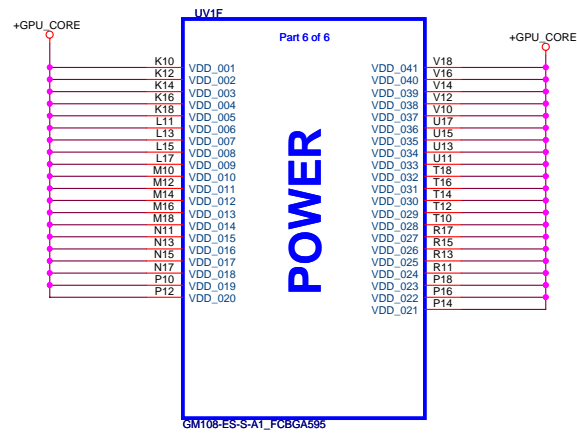
PEX\_IOVDD/Q Power Rail Combined

| Capacitor Type | Population |
|----------------|------------|
| 1uF 0402       | 1          |
| 4.7uF 0603     | 1          |
| 10uF 0805      | 1          |
| 22uF 0805      | 1          |

3.3V\_RUN\_GFX  
G05 2.0 G10/G12 pin connect to  
+3.3V\_FFX\_AON



Caps on Power Side  
1UX4 4.7UX10 under GPU  
4.7UX5 22UX1 47UX2 330UX2 near GPU



|   |                    |                 |            |                              |                |
|---|--------------------|-----------------|------------|------------------------------|----------------|
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|   |                    |                 |            | 4019RU                       | A              |
|   |                    |                 |            | Date: Monday, April 07, 2014 | Sheet 48 of 54 |



# GDDR3L CMD Mapping Table

DATA Bits[31..0] DATA Bits[63..32]

|       |      |  |
|-------|------|--|
| CMD0  | CS0# |  |
| CMD1  | ODT  |  |
| CMD2  | CKE  |  |
| CMD3  | CKE  |  |
| CMD4  | A14  |  |
| CMD5  | RST  |  |
| CMD6  | A9   |  |
| CMD7  | A7   |  |
| CMD8  | A2   |  |
| CMD9  | A0   |  |
| CMD10 | A4   |  |
| CMD11 | A1   |  |
| CMD12 | BA0  |  |
| CMD13 | WE#  |  |
| CMD14 | A15  |  |
| CMD15 | CAS# |  |
| CMD16 | CS0# |  |
| CMD17 | ODT  |  |
| CMD18 | CKE  |  |
| CMD19 | CKE  |  |
| CMD20 | A13  |  |
| CMD21 | A8   |  |
| CMD22 | A6   |  |
| CMD23 | A11  |  |
| CMD24 | A5   |  |
| CMD25 | A3   |  |
| CMD26 | BA2  |  |
| CMD27 | BA1  |  |
| CMD28 | A12  |  |
| CMD29 | A10  |  |
| CMD30 | RAS# |  |
| CMD31 |      |  |

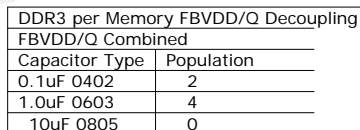
|         |      |         |
|---------|------|---------|
| FBA_D0  | E18  | FBA_D00 |
| FBA_D1  | F18  | FBA_D01 |
| FBA_D2  | E16  | FBA_D02 |
| FBA_D3  | F17  | FBA_D03 |
| FBA_D4  | D20  | FBA_D04 |
| FBA_D5  | D21  | FBA_D05 |
| FBA_D6  | F20  | FBA_D06 |
| FBA_D7  | E21  | FBA_D07 |
| FBA_D8  | E15  | FBA_D08 |
| FBA_D9  | D15  | FBA_D09 |
| FBA_D10 | F15  | FBA_D10 |
| FBA_D11 | F13  | FBA_D11 |
| FBA_D12 | C13  | FBA_D12 |
| FBA_D13 | B13  | FBA_D13 |
| FBA_D14 | E13  | FBA_D14 |
| FBA_D15 | D13  | FBA_D15 |
| FBA_D16 | B15  | FBA_D16 |
| FBA_D17 | C16  | FBA_D17 |
| FBA_D18 | A13  | FBA_D18 |
| FBA_D19 | A15  | FBA_D19 |
| FBA_D20 | B19  | FBA_D20 |
| FBA_D21 | A18  | FBA_D21 |
| FBA_D22 | A19  | FBA_D22 |
| FBA_D23 | C19  | FBA_D23 |
| FBA_D24 | B24  | FBA_D24 |
| FBA_D25 | C23  | FBA_D25 |
| FBA_D26 | A25  | FBA_D26 |
| FBA_D27 | A24  | FBA_D27 |
| FBA_D28 | A21  | FBA_D28 |
| FBA_D29 | B21  | FBA_D29 |
| FBA_D30 | C20  | FBA_D30 |
| FBA_D31 | C21  | FBA_D31 |
| FBA_D32 | R22  | FBA_D32 |
| FBA_D33 | R24  | FBA_D33 |
| FBA_D34 | T22  | FBA_D34 |
| FBA_D35 | R23  | FBA_D35 |
| FBA_D36 | N25  | FBA_D36 |
| FBA_D37 | N26  | FBA_D37 |
| FBA_D38 | N23  | FBA_D38 |
| FBA_D39 | N24  | FBA_D39 |
| FBA_D40 | V23  | FBA_D40 |
| FBA_D41 | V22  | FBA_D41 |
| FBA_D42 | T23  | FBA_D42 |
| FBA_D43 | U22  | FBA_D43 |
| FBA_D44 | Y24  | FBA_D44 |
| FBA_D45 | A24  | FBA_D45 |
| FBA_D46 | Y22  | FBA_D46 |
| FBA_D47 | AA23 | FBA_D47 |
| FBA_D48 | AD27 | FBA_D48 |
| FBA_D49 | AB25 | FBA_D49 |
| FBA_D50 | AD26 | FBA_D50 |
| FBA_D51 | AC25 | FBA_D51 |
| FBA_D52 | AA26 | FBA_D52 |
| FBA_D53 | W26  | FBA_D53 |
| FBA_D54 | Y25  | FBA_D54 |
| FBA_D55 | R26  | FBA_D55 |
| FBA_D56 | T25  | FBA_D56 |
| FBA_D57 | N27  | FBA_D57 |
| FBA_D58 | N27  | FBA_D58 |
| FBA_D59 | V26  | FBA_D59 |
| FBA_D60 | V27  | FBA_D60 |
| FBA_D61 | W27  | FBA_D61 |
| FBA_D62 | W25  | FBA_D62 |
| FBA_D63 | W25  | FBA_D63 |

UV18

Part 2 of 6

MEMORY INTERFACE A

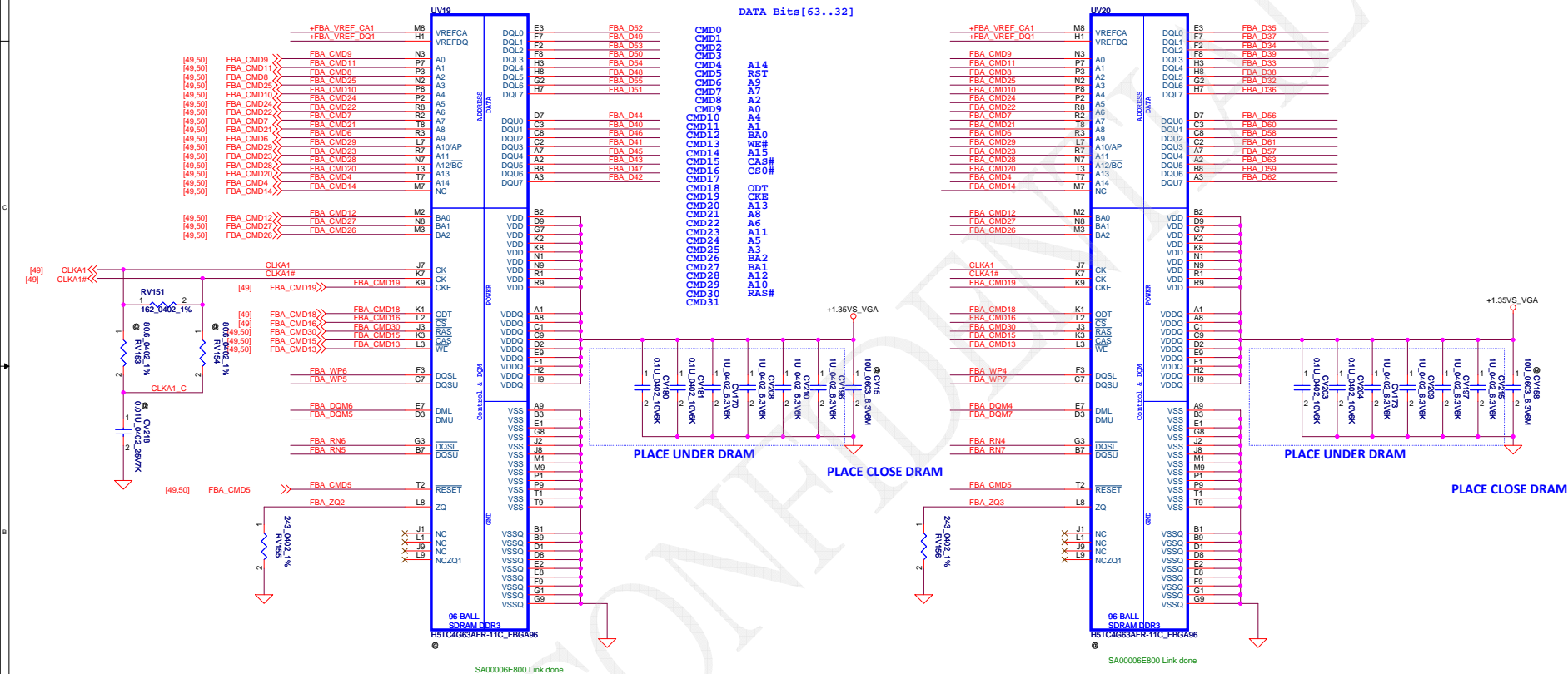
|            |     |           |               |         |
|------------|-----|-----------|---------------|---------|
| FBA_CMD0   | C27 |           | FBA_CMD0      | [50]    |
| FBA_CMD1   | C26 | FBA_CMD1  |               |         |
| FBA_CMD2   | E24 | FBA_CMD2  | ● T110 PAD-D@ |         |
| FBA_CMD3   | F24 | FBA_CMD3  |               |         |
| FBA_CMD4   | D27 |           | FBA_CMD4      | [50,51] |
| FBA_CMD5   | D26 | FBA_CMD5  |               |         |
| FBA_CMD6   | F25 |           | FBA_CMD6      | [50,51] |
| FBA_CMD7   | F26 |           | FBA_CMD7      | [50,51] |
| FBA_CMD8   | F23 |           | FBA_CMD8      | [50,51] |
| FBA_CMD9   | G22 |           | FBA_CMD9      | [50,51] |
| FBA_CMD10  | G23 |           | FBA_CMD10     | [50,51] |
| FBA_CMD11  | G24 |           | FBA_CMD11     | [50,51] |
| FBA_CMD12  | F27 |           | FBA_CMD12     | [50,51] |
| FBA_CMD13  | G25 |           | FBA_CMD13     | [50,51] |
| FBA_CMD14  | G27 |           | FBA_CMD14     | [50,51] |
| FBA_CMD15  | M24 |           | FBA_CMD15     | [50,51] |
| FBA_CMD16  | M23 | FBA_CMD17 |               |         |
| FBA_CMD17  | K24 | FBA_CMD18 | ● T183 PAD-D@ |         |
| FBA_CMD18  | K23 | FBA_CMD19 |               |         |
| FBA_CMD19  | M26 |           | FBA_CMD19     | [51]    |
| FBA_CMD20  | M27 |           | FBA_CMD20     | [50,51] |
| FBA_CMD21  | M25 |           | FBA_CMD21     | [50,51] |
| FBA_CMD22  | K26 |           | FBA_CMD22     | [50,51] |
| FBA_CMD23  | K22 |           | FBA_CMD23     | [50,51] |
| FBA_CMD24  | J23 |           | FBA_CMD24     | [50,51] |
| FBA_CMD25  | J25 |           | FBA_CMD25     | [50,51] |
| FBA_CMD26  | J24 |           | FBA_CMD26     | [50,51] |
| FBA_CMD27  | K27 |           | FBA_CMD27     | [50,51] |
| FBA_CMD28  | K25 |           | FBA_CMD28     | [50,51] |
| FBA_CMD29  | J27 |           | FBA_CMD29     | [50,51] |
| FBA_CMD30  | J26 | FBA_CMD31 | ● T184 PAD-D@ |         |
| FBA_CMD31  |     |           |               |         |
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| Title                           | <b>SCHEAMTICS,MB AB072</b> |          |  |
| Size                            | Document Number            | Revision |  |
|                                 | <b>4019RU</b>              |          |  |

FBA\_D[32..63] <<> FBA\_D[32..63] [49]  
 FBA\_WP[4..7] <<> FBA\_WP[4..7] [49]  
 FBA\_DOM[4..7] <<> FBA\_DOM[4..7] [49]  
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| Item | Page#          | Title                | Date       | Request Owner | Issue Description                                 | Solution Description   | Rev. |
|------|----------------|----------------------|------------|---------------|---|--|------|
| 1    | 31             | KB control           | 2013/10/21 | EE            | Change Fuse package for sales suggestion          | Change F1 From SP040003E00 to SP040003A00  | X01  |
| 2    | 23             | Audio Codec ALC3234  | 2013/10/21 | EE            | fix POP noise issue                               | Add RAl129 from 100K to UAl pin 27, and NC RC366   | X01  |
| 3    | ALL            | ALL                  | 2013/10/21 | EE            | Re-name part of connector                         | JCRT1 --> JCRT, JAP51 --> JAPS, JDEG1 --> JDEG, JLPDE1 --> JLPDE, JKB1 --> JKB, JNGFF1 --> JNGFF<br>JXDP1 --> JXDP, JRTCL --> JRTC, PJPDC1 --> JDCIN, PBATT1 --> JBATT   | X01  |
| 4    | ALL            | ALL                  | 2013/10/21 | EE            | Re-name part of jump                              | PJ200 --> PJP200, PJ201 --> PJP201, PJ203 --> PJP203, PJ400 --> PJP400, PJ401 --> PJP401, JP12 --> PJP12<br>JP13 --> PJP13, J510 --> PJP510, J511 --> PJP511, J512 --> PJP512, J513 --> PJP513, PJ1000 --> PJP1000 |      |
| 5    | 23             | Audio Codec ALC3234  | 2013/10/23 | EE            | Update P/N for X1 code issue                      | Change LA8, LA9 form SM010018110 to SM01000E100  |      |
| 6    | 1              | Cover page           | 2013/10/28 | EE            | Add Micron sku for X76 level                      | Add UV17, UV18, UV19, UV20 for SA000077K0L, RV59 for 24.9K   | X01  |
| 7    | 27             | LED/DB               | 2013/10/29 | EE            | delete circuit for EC control LED blink issue     | Delete Q2417   |      |
| 8    | 29             | KBC & GPIO MEC5085   | 2013/10/31 | EE            | Depop item by EC request                          | Depop RE278  |      |
| 9    | 22             | LAN RTL8111GUS-CG    | 2013/10/31 | EE            | Change Power switch for cost down plan            | Change UL2 from SA00003AR00 to SA000079400, Delete CL38, Add RL41  | X01  |
| 10   | 21             | eDP/webcam/touch     | 2013/10/31 | EE            | Change Power switch for cost down plan            | Change UX1, UX3 from SA00003AR00 to SA000079400, Delete CX9, CX52, Add RX30, RX31 to 100K  | X01  |
| 11   | 31             | DC/DC interface      | 2013/10/31 | EE            | Change Load switch for cost down plan             | Change U2301, U2304 from SA00004MM00 to SA00006FD00  | X01  |
| 12   | 50             | N15S-MEM Interface A | 2013/10/31 | EE            | Change Load switch for cost down plan             | Change UV15 from SA00004MM00 to SA00006FD00  | X01  |
| 13   | 25             | NGFF_WLAN            | 2013/10/31 | EE            | Change Power switch for cost down plan            | Change UM1 from SA00005XM00 to SA000070L00, Add CM8 to 2200P   | X01  |
| 14   | 22             | LAN RTL8111GUS-CG    | 2013/10/31 | EE            | Change Transformer for cost down plan             | Change TL2 from SP050007Q00 to SP050006P00   | X01  |
| 15   | 20             | DP to CRT            | 2013/11/05 | EE            | Add cap for reduce power ripple by vendor confirm | Add CV361 to 22uF and close UV6 pin 38   | X01  |
| 16   | 23             | Audio Codec ALC3234  | 2013/11/05 | EE            | Add capacitor for codec stable                    | Add CA77 to 4.7uF_0603 and close UAl pin36   |      |
| 17   | 19, 24, 26, 27 | Common mode Choke    | 2013/11/12 | EE            | Change Common mode choke for X1 code              | Change LI2, LX2, LI2, LX3, LX4, LX5, LI5, LX6, LX7, LI9, LI10 from SM070001S00 to SM070003Y00<br>Change LI1, LI3, LI4, LI6 from SM070001R00 to SM070003Q00   | X01  |
| 18   | 27             | LED/DB               | 2013/11/12 | EE            | Delete MB common mode choke by EA measure         | Delete LI9, LI10   | X01  |
| 19   | 46             | N15S-PCIE            | 2013/11/13 | EE            | change bead for X1 code                           | Change LV8 from SM010028480 to SM010004700   | X01  |
| 20   | 24, 27         | USB                  | 2013/11/13 | EE            | Change USB I/O power switch for Cost down         | Change UI2, UI3, UI4 from SA00003XM00 to SA00007AO00, Delete CI7, CI14, CI18, CI45, Change CI6, CI12, CI44 from 4.7U_0805 to 1U_0603   |      |
| 21   | 13, 17         | Buffer output        | 2013/11/13 | EE            | change buffer output for cost down                | Change UC6, U2303 from SA00005U600 to SA00007KJ00  | X01  |
| 22   | 46             | N15S-PCIE            | 2013/11/14 | EE            | change AND gate for cost down                     | Change UV14 from SA007080120 to SA00000OH00  | X01  |
| 23   | 17, 27, 30     | DDR & LED & KB       | 2013/11/14 | EE            | change MOSFET for cost down                       | Change Q12, QE11, Q327 from SB00000U000 to SB00000ST00, Change QD2 from SB501380050 to SB00000ST00   | X01  |
| 24   | 23             | Audio Codec ALC3234  | 2013/11/15 | EE            | modify by EMC request                             | Change RAl126, RAl127 to SM01000FG00, Change CA38, CA40 from 100p to 680p  | X01  |
| 25   | 46, 50         | N15S-PCIE            | 2013/11/15 | EE            | modify for GPU power sequence                     | Change RV45 from pull high to 45.3K pull down, Depop CV141, Change CV140 from 470P to 1000P  |      |
| 26   | 23             | Audio Codec ALC3234  | 2013/11/18 | EE            | Change EMI solution                               | Change RAl121, RAl122, RAl123, RAl124 from 0 ohm to SM01000NO00  | X01  |
| 27   | 29             | KBC & GPIO MEC5085   | 2013/11/18 | EE            | Add ESD diode by EMC request                      | Add DE2 for PECCI_EC net   |      |
| 28   | 26             | HDD/Finger print     | 2013/11/19 | EE            | Rename Location                                   | Re-name U2413 to DS1   |      |
| 29   | 08, 29         | Crystal              | 2013/11/20 | EE            | Crystal fine tune                                 | Change CE53 from 22P to 27P  |      |
| 30   | 20             | DP to CRT            | 2013/11/21 | EE            | Add Power pin connect to power by vendor          | Add RV518 10K to +3VS_VGA  |      |
| 31   | 21             | eDP/ HDD / PAD       | 2013/11/21 | EE            | change connector & PAD by ME                      | Change JEDP to SP010013I00, JHDD to SP02000TR00, H1, H2, H15, H24 update footprint   |      |
| 32   | 23, 26         | Audio & Finger       | 2013/11/21 | EE            | modify by EMC request                             | Change LA8, LA9 from SM010018110 to SM01000MJ00, Change RS39 from 0603 to 0402   |      |
| 33   | 27             | ESD                  | 2013/11/21 | EE            | ESD BOM slim plan                                 | Change DE1, DV5, DV6 to SCA00001L00,   |      |
| 34   | 21             | Camera               | 2013/11/21 | EE            | Camera voltage drop                               | Delete RX27, Add QX5 and Change +3VS to +3VALW   |      |
| 35   | 23             | Audio                | 2013/11/25 | EE            | Change ESD diode by EMC request                   | Change DA12 to SC400007Q00, Add DA14 to SC400007Q00  |      |
| 36   | 46             | N15S-PCIE            | 2013/11/26 | EE            | Add diode for prevent leakage                     | Add DV9 for GC6_EVENT#   |      |
| 37   | 32             | Screw Hole           | 2013/11/26 | EE            | Modify Screw hole by ME update DXF                | Delete H13, H18, Add H24   |      |
| 38   | 29             | KBC & GPIO MEC5085   | 2013/11/27 | EE            | Change Connector for ME issue                     | Change JDEG from SP01001FP00 to SP01001L100, Change JLPDE from SP01001FP00 to SP01000HE00  |      |
| 39   | 21             | eDP                  | 2013/11/27 | EE            | Add EMI solution for eDP                          | Add LX8, LX9, LX10, for SM070003Q00, Add RX32, RX33, RX34, RX35, RX36, RX37 for 0 ohm  |      |
| 40   | 29             | KBC & GPIO MEC5085   | 2013/11/27 | EE            | Change Resistor for Thermal request               | Change RE77 from 1.58K to 1.96K  |      |
| 41   | 46             | N15S-PCIE            | 2013/11/28 | EE            | GPU circuit modify by vendor feedback             | Add RV519 for GPU_CLK_27M_OUT, pop DV8, RV29, reserve RV208, Change power for ROM_SO_GPU/ROM_SI_GPU/ROM_SCLK_GPU   |      |

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## Version Change List (P. I. R. List)

## Page 1

| Item | Page# | Title                | Date       | Request Owner | Issue Description                                   | Solution Description   | Rev. |
|------|-------|----------------------|------------|---------------|---|--|------|
| 1    | P40   | PROCESSOR DECOUPLING | 2013/11/12 | PWR           | SSI verify , Vcore keep 18 keep                     | PC901,PC907,PC923,PC912,PC903 change from pop to de-pop  |      |
| 2    | P41   | Charger_BQ24777      | 2013/11/12 | PWR           | EMI requirement                                     | Pc723,PC724,PC725 change from de-pop to pop  |      |
| 3    | P33   | DCIN/BATT CONN/OTP   | 2013/11/12 | PWR           | EMI requirement                                     | Add PL5/PL7(SM01000C000)   |      |
| 4    | P33   | DCIN/BATT CONN/OTP   | 2013/11/12 | PWR           | EMI requirement                                     | Add PL8(SM01000C000), PL1/PL2/PL5/PL6 change from SM010009C80 to SM01000C000 for finding 2nd source easily |      |
| 5    | P33   | VCORE                | 2013/11/12 | PWR           | EMI requirement                                     | PL502 change from 0.22uH to 0.15uH   |      |
| 6    | P38   | VCORE                | 2013/11/12 | PWR           | Vcore test result abjustmet value                   | PR521 change from 97.6k to 95.3k   |      |
| 7    | P38   | VCORE                | 2013/11/12 | PWR           | change to Vendor ( CYNTEC)                          | PL502 change to SH00000PQ00  |      |
| 8    | P38   | VCORE                | 2013/11/12 | PWR           | EMI requirement                                     | add PL504(SM01000C000)   |      |
| 9    | P38   | VCORE                | 2013/11/12 | PWR           | for common part                                     | PL501 change from SM010009C80 to SM01000C000   |      |
| 10   | P34   | 3.3VALWP/SVALWP      | 2013/11/13 | PWR           | for common part                                     | PL100 change from SH00000MS00 to SH00000YC00   |      |
| 11   | P37   | +1.35VP/0.675VSP     | 2013/11/13 | PWR           | for common part                                     | PL200 change from SH00000KS00 to SH00000YE00   |      |
| 12   | P45   | +1.35VGPU_DDR        | 2013/11/13 | PWR           | for common part                                     | PL1001 change from SH00000MR00 to SH00000YV00  |      |
| 13   | P38   | VCORE                | 2013/11/14 | PWR           | Vcore test result abjustmet value                   | PR521 change from 95.3k to 90.9k   |      |
| 14   | P39   | +VCCIO               | 2013/11/15 | PWR           | for common part                                     | PL302 change form SM010009C80 to SM01000C000   |      |
| 15   | P33   | DCIN/BATT CONN/OTP   | 2013/11/21 | PWR           | ESD requirement                                     | add PD3 (AZ5125-01H.R7G_SOD523-2)  |      |
| 16   | P34   | 3.3VALWP/SVALWP      | 2013/11/21 | PWR           | change to same material                             | PD101 change from SCA00002A00 to SCA00001W00   |      |
| 17   | P41   | Charger_BQ24777      | 2013/11/21 | PWR           | peak shift issue                                    | Add PQ709  |      |
| 18   | P44   | VGA_COREP            | 2013/11/21 | PWR           | ocp modify to 66A                                   | PR615 change from 10.7k to 13k   |      |
| 19   | P38   | VCORE                | 2013/11/25 | PWR           | current rating issue                                | PC520 change from 0402 to 0603   |      |
| 20   | P41   | Charger_BQ24777      | 2013/11/26 | PWR           | check circuit modify error                          | PQ708A swap pin1 and pin6  |      |
| 21   | P39   | +VCCIO               | 2013/11/28 | PWR           | for buyer suggest change material                   | PR303 chang from SD00001FX00 to SD013000080  |      |
| 22   | P43   | Charger_BQ24777      | 2013/11/28 | PWR           | Vendor spec BQ24777_REGN modify to 5.4V             | R715 change from 121k to 154k  |      |
| 23   | P38   | VCORE                | 2013/12/04 | PWR           | DFB issue   | remove PL503   |      |
| 24   | P41   | Charger_BQ24777      | 2014/2/17  | PWR           | peak shift issue                                    | PR729 NC   |      |
| 25   | P41   | Charger_BQ24777      | 2014/2/17  | PWR           | PIN21 change from NC to input current limit mode    | add PR706 10Kohm and pull high   |      |
| 26   | P41   | Charger_BQ24777      | 2014/2/17  | PWR           | leakage current issue                               | change PD701(SCS00003800) to PD702,PD703(SCS0340L010)  |      |
| 27   | P41   | Charger_BQ24777      | 2014/2/17  | PWR           | PIN9 change from Voltage monitor to current monitor | change PC753(100P) to PR732 (20K)  |      |
| 28   | P38   | VCORE                | 2014/2/17  | PWR           | Vcore test result abjustmet value                   | PR535 change from 210 to 200   |      |
| 29   | P43   | VGA_COREP            | 2014/2/17  | PWR           | ME Z-High issue                                     | PC604 change from pop to de-pop,PC627 change from de-pop to pop  |      |
| 30   | P33   | DCIN/BATT CONN/OTP   | 2014/2/17  | PWR           | hiccup mode issue                                   | add Erp lot 6 circuit  |      |
| 31   | P41   | Charger_BQ24777      | 2014/2/21  | PWR           | plug Adapter system no work issue                   | add PR741 connect PQ709 Gate to GND  |      |
| 32   | P44   | +1.35VGPU_DDR        | 2014/3/4   | PWR           | for EE suggest                                      | net name change from FBVDD_EN to GFX_CORE_PG   |      |
| 33   | P41   | Charger_BQ24777      | 2014/3/5   | PWR           | acoustic noise                                      | add PC730,PC731,PC732 to de-pop  |      |
| 34   | P41   | Charger_BQ24777      | 2014/3/11  | PWR           | Follow Houston test summary solution NC             | PQ708A,PQ708B NC   |      |
| 34   | P38   | VCORE                | 2014/3/11  | PWR           | acoustic noise                                      | Change PC515 PC533 from VCC_PWR_SRC to B+  |      |
| 35   | P37   | +1.35VP/0.675VSP     | 2014/3/14  | PWR           | select the correct voltage to 2.5V                  | PC214 change from SF000003000 to SF000003100   |      |
| 36   | P33   | DCIN/BATT CONN/OTP   | 2014/3/17  | PWR           | hiccup mode issue                                   | add PR13 NC  |      |
| 37   | P34   | 3.3VALWP/SVALWP      | 2014/3/17  | PWR           | Co-Lay  | add PC116 PC117 NC   |      |
| 38   | P41   | Charger_BQ24777      | 2014/3/17  | PWR           | follow TI solution                                  | change PR725 from 100K to 1K   |      |
| 39   | P41   | Charger_BQ24777      | 2014/3/21  | PWR           | hiccup mode issue                                   | change PR739 from 316K to 294K   |      |
| 40   | P34   | 3.3VALWP/SVALWP      | 2014/3/24  | PWR           | follow EC solution                                  | PR110 NC   |      |

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